



# Designing with the Ultra-Low Power Intel486™ SX Processor

Application Note

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## 1.0 Introduction

This application note will assist in the development of embedded applications using the Ultra-Low Power Intel486™ SX processor, which is suited for low-power operation. This application note includes descriptions of components that can be used with the Ultra-Low Power (ULP) Intel486 SX processor. Features for common applications include connectors for in-circuit emulation, jumper-selectable frequency and voltage options, a flash device with system software, an ISA edgeboard connector, and infrared sensors.

The key components discussed include the ULP Intel486 SX processor, Intel flash memory, a Chips & Technologies graphics accelerator and the Radisys R400EX\* companion chip. These are not recommendations and designs are not limited to these components.

**Note:** Schematics from a sample design are provided to use as a guideline for implementing the features discussed in this application note. The sample design has not been implemented in hardware. The design suggests one possible implementation. It is up to the designer to verify any designs based on the sample schematics provided.

## 2.0 System Overview

Embedded systems using the ULP Intel486 SX processor can use the Radisys R400EX embedded system controller to perform system control and I/O functions. A traditional processor evaluation board providing an environment for code execution, debug and hardware development can be built by referring to the schematics provided. This design is also valuable when used within an embedded PC environment where applications are written on top of a PC-like BIOS and ROMable Operating System. Additional functionality can be incorporated within a customer-specific prototype or development environment. New embedded designs can get to market sooner by taking advantage of the PC infrastructure for both hardware and software development. When equipped with a BIOS and a ROMable OS there is no need to build an embedded application from scratch. A system can include keyboard and mouse interface, an IDE drive interface, floppy disk drive interface, an ISA interface, and LCD/VGA display capabilities.

To enable embedded systems based on any of the embedded Intel486 processor family members, a 168-pin PGA socket should be designed into the board. By setting or removing jumpers, the user can disable the ULP Intel486 SX processor and enable the processor installed in the upgrade socket. To use the upgrade socket, place a jumper on the RESERVED#<sup>1</sup> signal. When the RESERVED# signal is active, the processor becomes disabled and is transparent to the rest of the system. Using this method, a system designer can design one board that supports the entire embedded Intel486 family of processors.

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1. See the *Embedded Ultra-Low Power Intel486™ SX Processor* datasheet (order number 272731) for information on the RESERVED# pin.

## 3.0 Component Overview

### 3.1 Chips & Technologies 65550\* Graphics Accelerator

The 65550 Graphics Accelerator is a highly integrated flat panel and CRT GUI accelerator and multimedia engine, palette/DAC, and clock synthesizer. The 65550 supports PCI, VL-Bus and 486 Local Bus protocols.

The 65550 supports various memory configurations through a 32-bit memory interface. The design uses four 256 Kx16 FPM DRAM devices providing a total of 2 Mbytes of video DRAM. Other memory configurations supported include:

- Two 256 Kx16 DRAMs
- One 512 Kx32 DRAM
- Two 128 Kx32 DRAMs
- Four 128 Kx16 DRAMs

Video BIOS is integrated into the system BIOS. 16 Mbytes of DRAM is supported.

### 3.2 Intel's 28F400BV, 28F320S5 Flash Memory

Intel's 4-Mbit Smart Voltage Boot Block (28F400BV) flash memory is recommended for storing the system BIOS and video BIOS. Intel's Word-Wide FlashFile (28F320S5) memory is recommended for use as a Resident Flash Array (RFA). Designers can evaluate two types of flash storage: RFA for onboard solid state disk or flash PC Card for removable storage.

The Word-Wide FlashFile memory family maintains basic compatibility with Intel's 28F016SA and 28F016SV. Key enhancements include:

- Common Flash Interface (CFI) support
- Scalable Command Set (SCS) support
- Enhanced Suspend capabilities

These flash memory devices share a compatible Status Register, basic software commands, and pinout. The similarities enable a clean migration from the 28F016SA or 28F016SV. When upgrading, it is important to note that because of new features and density options, the devices have different device identifier codes. This allows for software optimization.

### 3.3 Radisys R400EX System Controller

The R400EX system controller, available in a 208-pin PQFP, is designed specifically to support Intel486 processors. It is an embedded chipset that addresses the functional needs of embedded applications. It is a single-chip solution that incorporates features used in most designs. It provides a simple, low-cost, glueless interface to additional chips, such as a full PC keyboard, a video controller, or a PCMCIA controller.

The functional design of the R400EX system controller is based on PC architecture. The DRAM controller is compatible with both Fast-Page-Mode (FPM) and Extended-Data-Out (EDO) DRAM. The keyboard/mouse controller and real-time clock are PC-compatible. The enhanced IDE interface supports a maximum transfer rate of 7.33 Mbytes per second. The ISA bus controller has a separate data bus, and manages the ISA signals to ensure a quiet bus for cycles not directed to the ISA address space.

The R400EX features include

- Supports Intel486 processors including the ULP Intel486 SX, IntelDX2™ and IntelDX4™ processors
- EDO/FPM DRAM controller supports from 1 Mbyte to 128 Mbytes
- Supports L1 write-back cache
- Two integrated 16550-compatible UARTs
- Integrated real-time clock
- Enhanced IDE interface or DRAM parity support
- Keyboard and mouse controller
- Power management
- SMI support
- 5 V or 3.3 V operation
- Complete PC-engine logic
- Supports seven PC-compatible DMA channels
- Supports fifteen PC-compatible ISA bus interrupts
- Integrated 8254-compatible timer/counter
- Supports local bus and ISA bus peripherals
- Four programmable I/O chip selects
- ROM or flash ROM interface
- BIOS shadowing
- Speaker interface
- Watchdog timer

The power-management capabilities of the R400EX system controller include clock-source switching, halt detection, SMI event generation, and a programmable clock-restart delay. The processor clock source can be switched between the CLK2OSC input and the 32.768 KHz real-time clock oscillator to reduce power consumption.

### 3.4 XC5200

The XC5200 delivers a solution for high-density, reprogrammable logic designs. Please refer to *Design Migration from XC4000 to XC5200* on the Xilinx web-site ([www.xilinx.com](http://www.xilinx.com)) for recommendations on using the XC5200 architecture.

### **3.5 LCD/VGA**

The Chips & Technologies 65550 Graphics Accelerator provides local bus graphic support. Both LCDs and CRTs are supported with varying resolutions. VGA uses a standard DB15 connector. LCDs can be attached using a 50-pin high-density header.

## **4.0 Sample Design System Features**

### **4.1 PCMCIA, IDE and Floppy Control**

An onboard single-slot Type II PCMCIA controller can provide access to PCMCIA modules and support large file transfers using portable media. A 40-pin IDE header enables booting the embedded design from an IDE-controlled hard drive. A floppy disk allows easy installation of software and copying of files.

### **4.2 Power Requirements and Operational Time/Life**

Multiple power supply options can easily be supported. Power to the board may be supplied by either a standard PC power supply, the ISA edgeboard connector, or a portable external power supply. A 3 Volt Lithium coin-cell battery can be used for the RTC and CMOS RAM.

- Obtain power from a 120 Volt, 60 Hz outlet with input tolerance of 115 to 230 Volts, 50 to 60 Hz, and 4 to 7 Amps. A converted 5 Volt signal should be used for the  $V_{CC}$  signal on the board. The 12 Volt signal can be used for programming the flash devices.
- An ISA edgeboard connector can provide the  $V_{CC}$  signal to power the board.
- A 3 Volt Lithium coin-cell battery should be socketed onto the board to provide backup power for the real-time clock (RTC) and CMOS RAM.

### **4.3 Infrared**

Two-way wireless communication can be supported using infrared (IR) as a transmission medium. The IrDA IR implementation allows serial communication at baud rates up to 115 Kbaud.

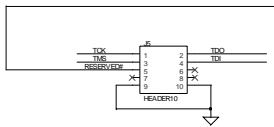
### **4.4 Hardware Interface**

In addition to the embedded PC hardware, various common embedded applications can also be integrated such as seven segment displays, and LCD support.

## **5.0 Sample Design Schematics**

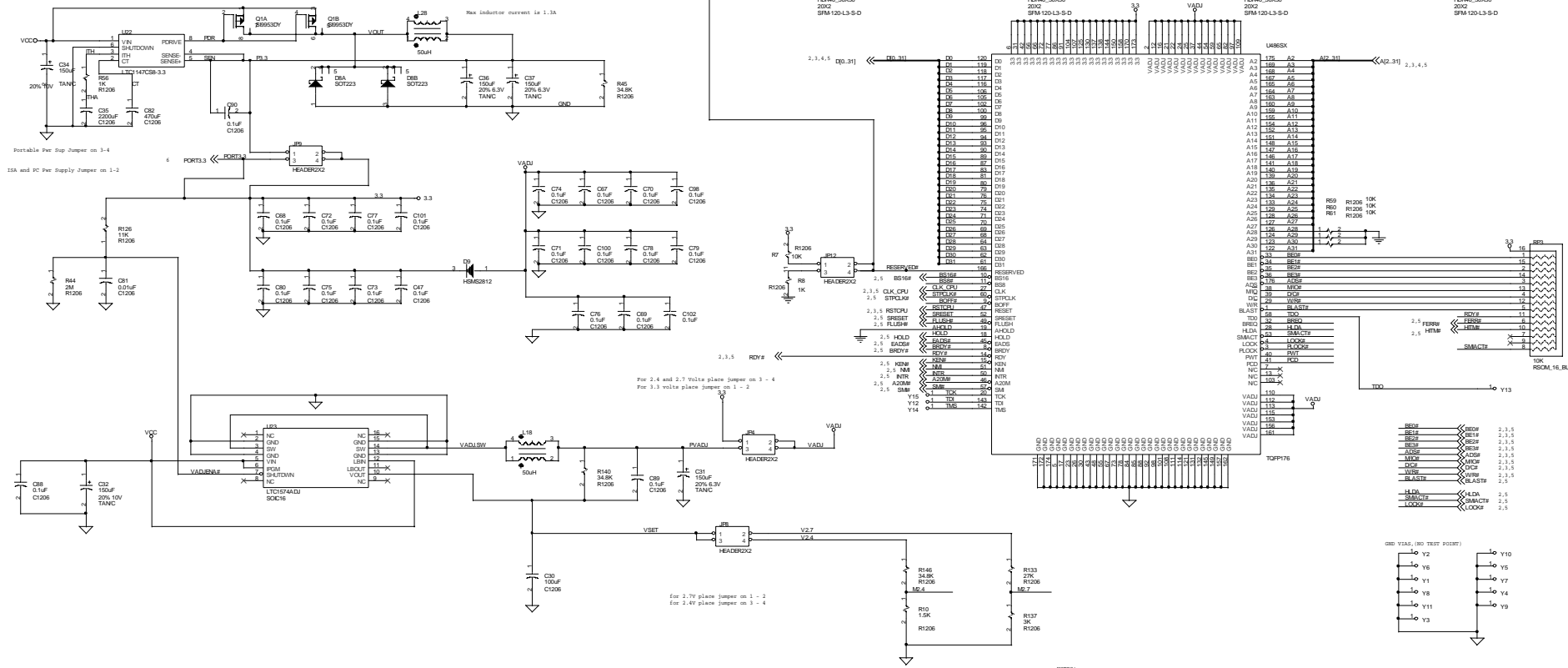
The following schematics are for reference only. This design has not been validated. It is up to the designer to validate any design based on these schematics.

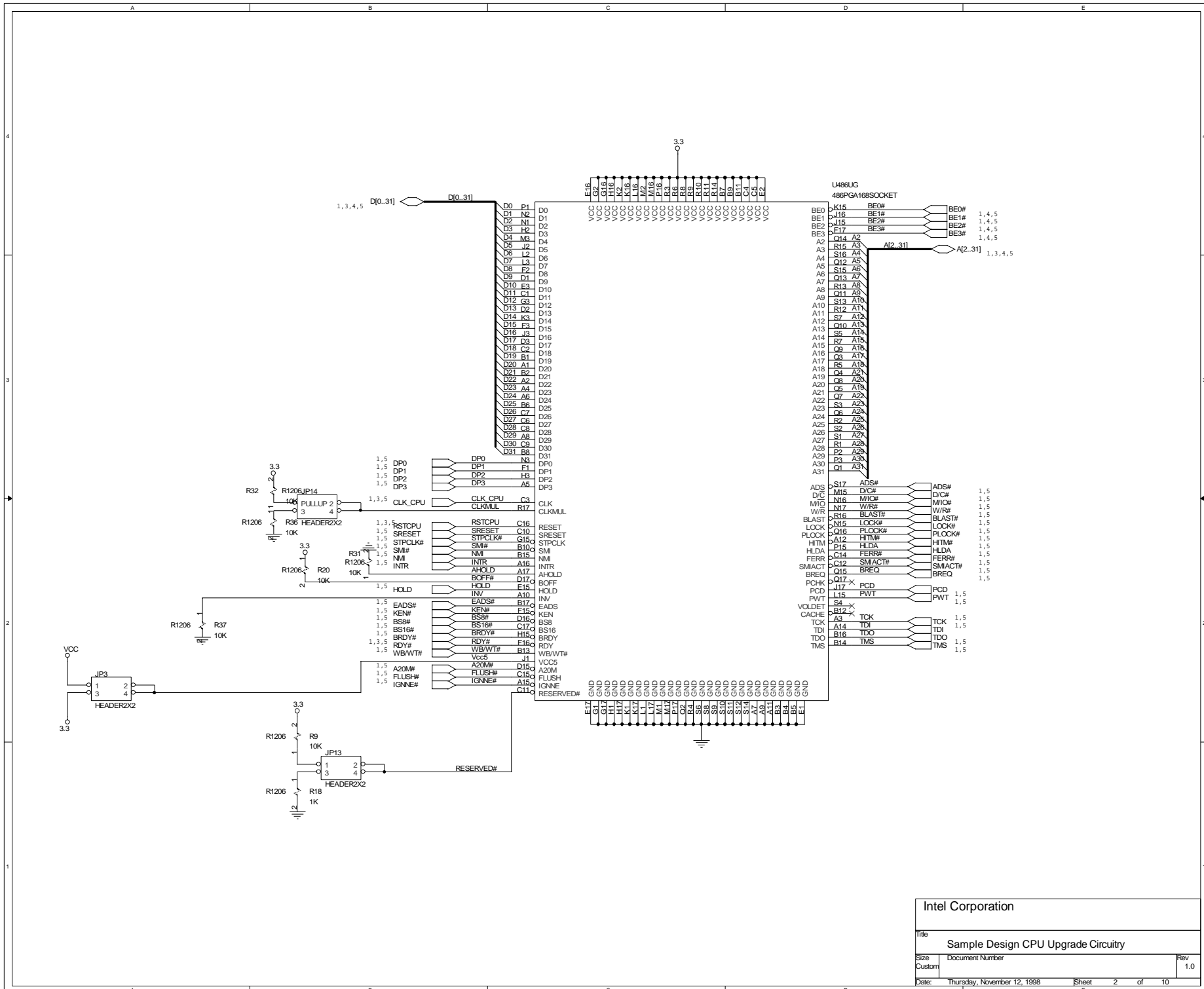


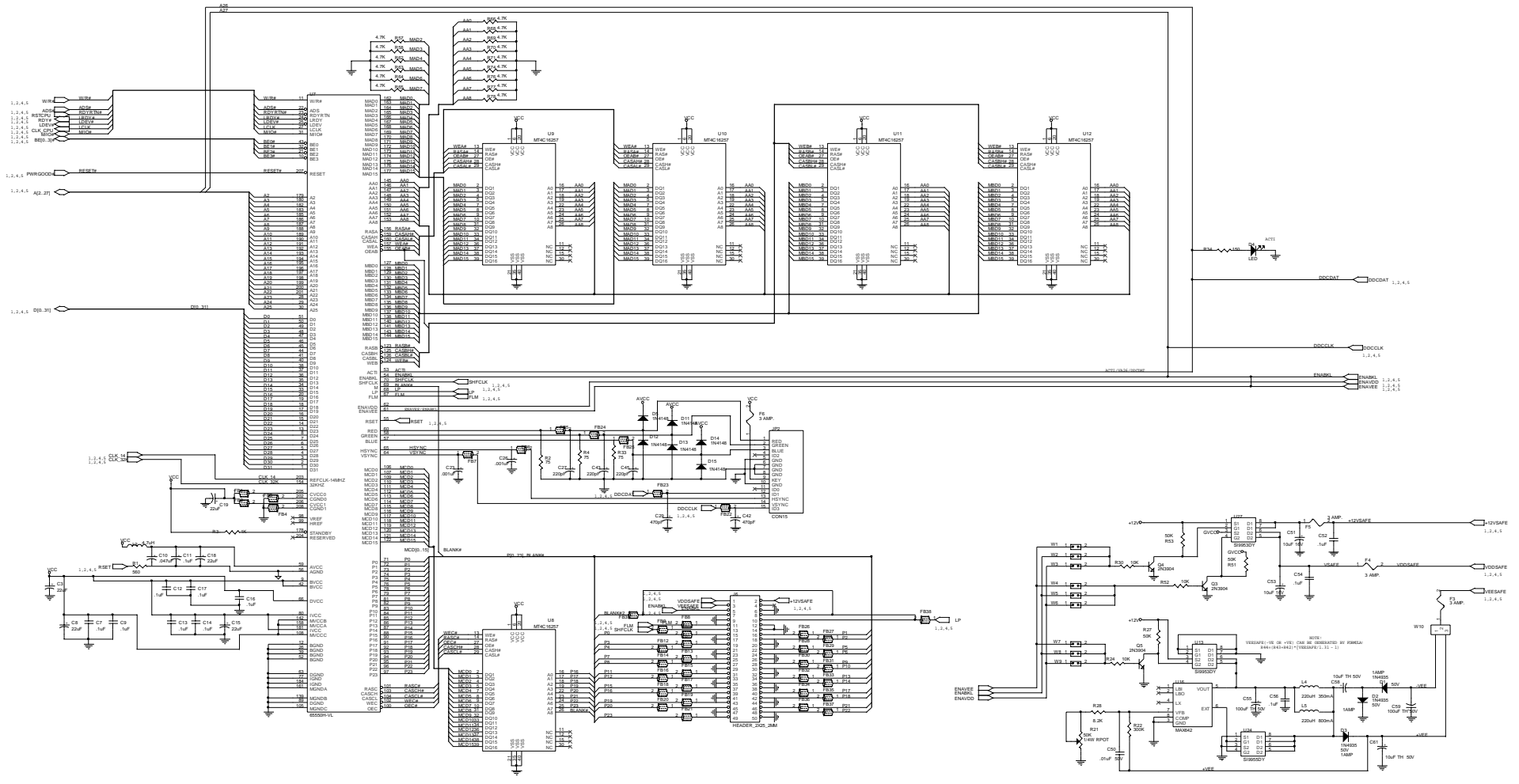


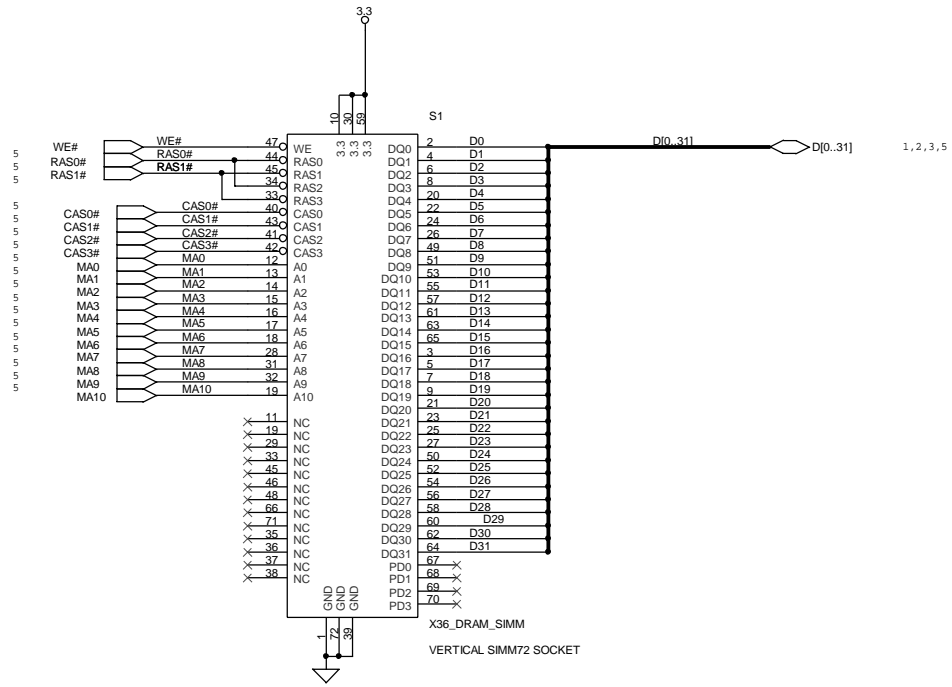
1" Dual-in-Line Header

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VADJ	1	RESV	1	AS	1	RESV	1	RESV
2	RESV	2	VADJ	2	AS	2	RESV	2	RESV
3	RESV	3	RESV	3	AS	3	RESV	3	RESV
4	RESV	4	RESV	4	AS	4	RESV	4	RESV
5	RESV	5	RESV	5	AS	5	RESV	5	RESV
6	RESV	6	RESV	6	AS	6	RESV	6	RESV
7	RESV	7	RESV	7	AS	7	RESV	7	RESV
8	RESV	8	RESV	8	AS	8	RESV	8	RESV
9	RESV	9	RESV	9	AS	9	RESV	9	RESV
10	RESV	10	RESV	10	AS	10	RESV	10	RESV





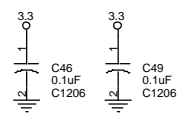




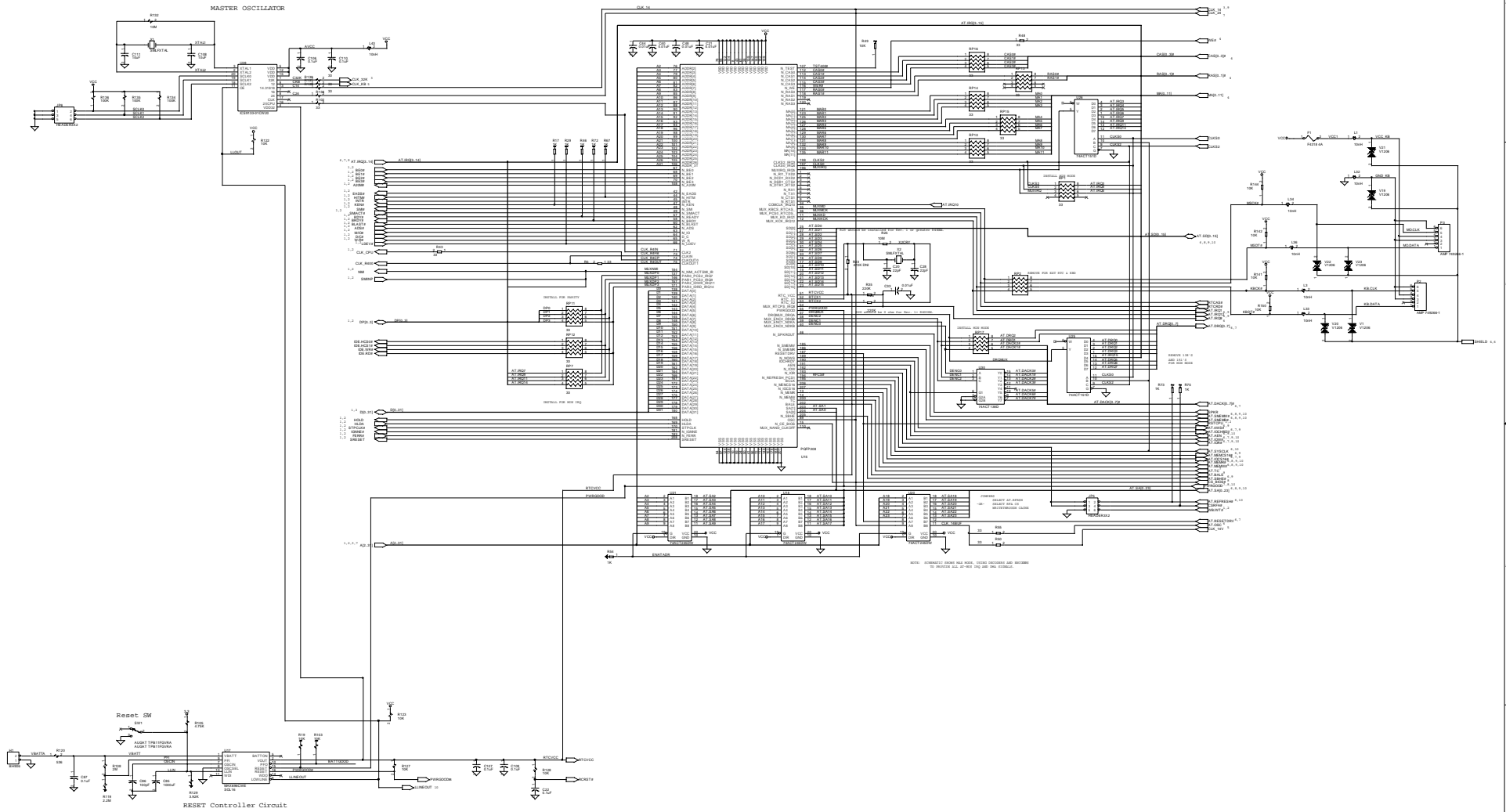
**DRAM SOCKET**

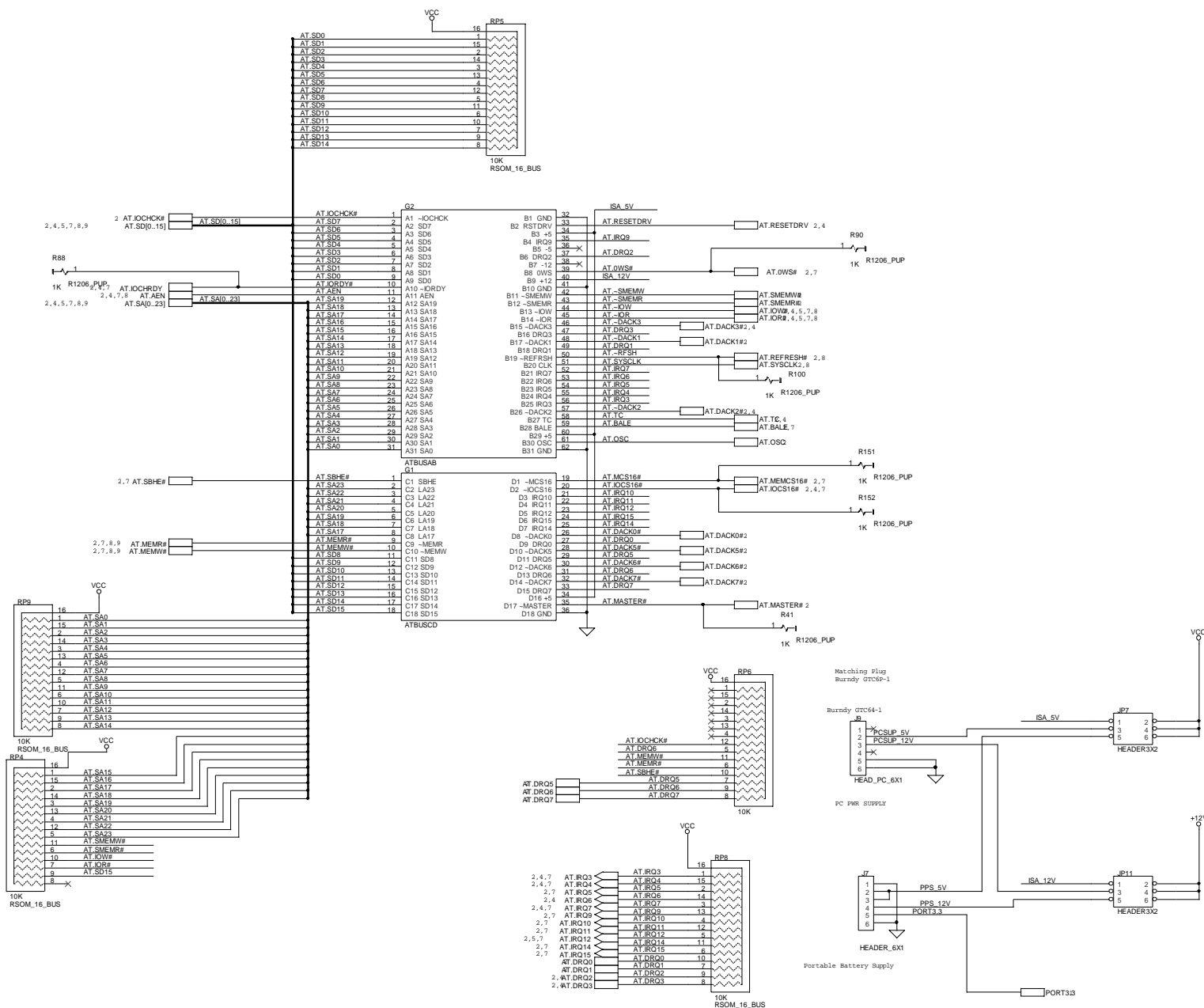
Socket Closest to Edge of Board

Power Supply for SIMM Sockets is +3.3 Volts



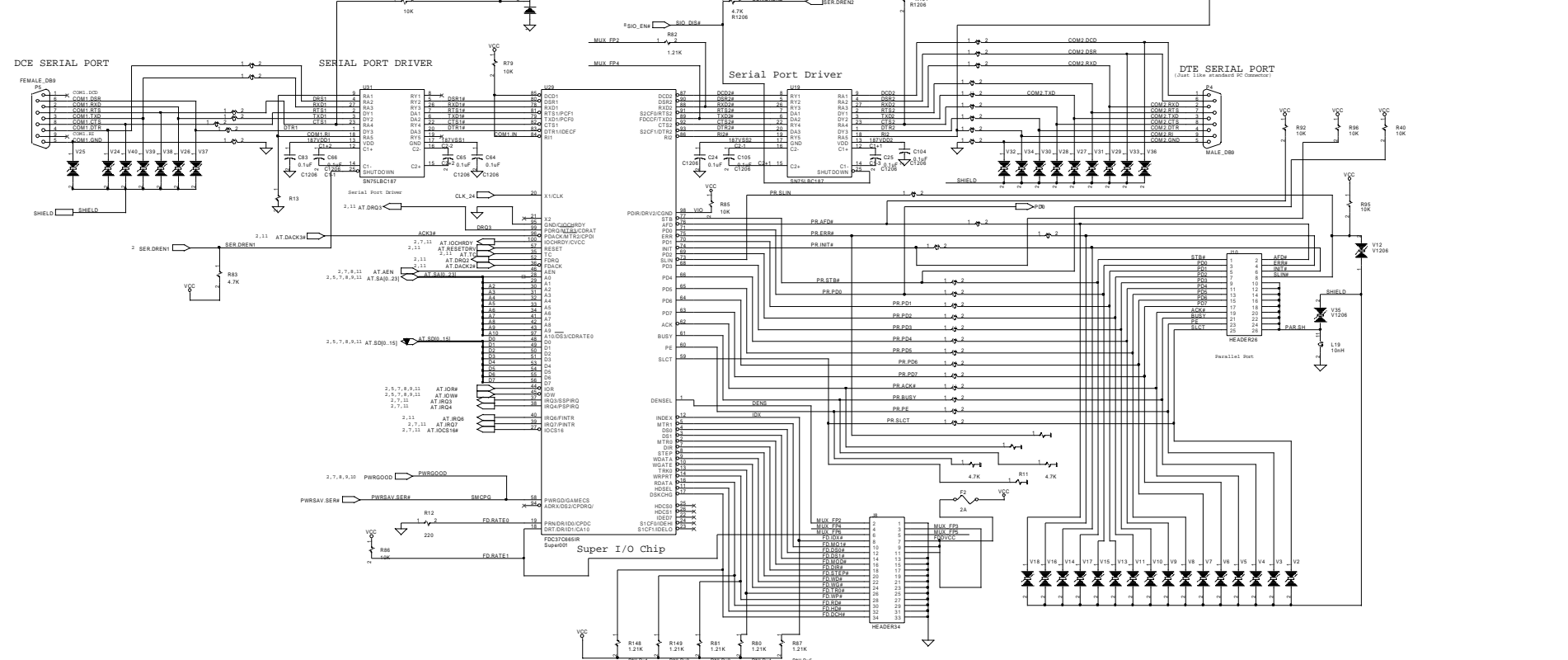
Intel Corporation		
Title Sample Design DRAM Circuitry		
Size B	Document Number	Rev 1.0
Date:	Thursday, November 12, 1998	Sheet 4 of 10



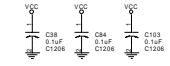




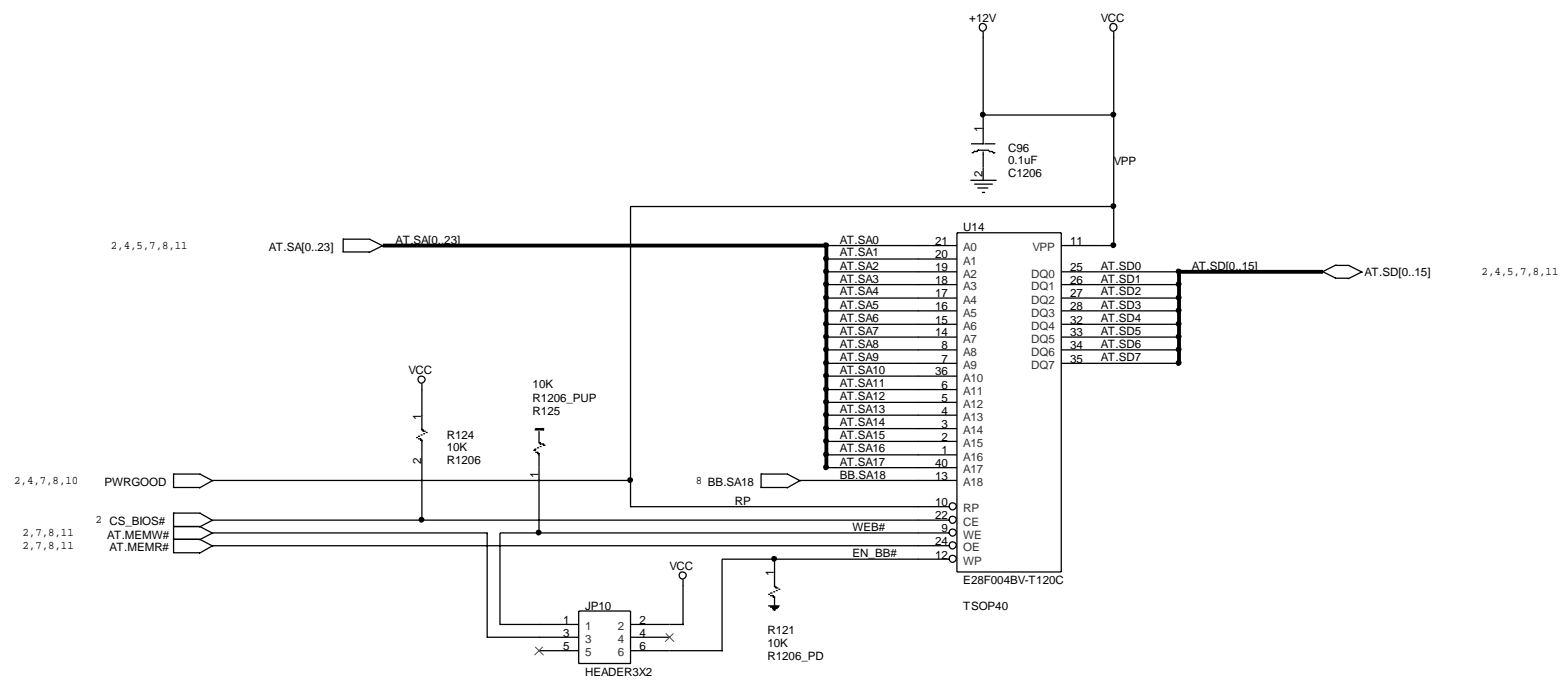
On a DCE Port the RXD/TXD, CTS/RTS and DSR/DSR are swapped.  
 Thus the DSR signal from a DCE port is an output and the TXD signal is an input.



Power Supply = +5 Volts  
 VCC is +5 Volt Plane

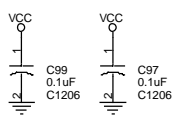


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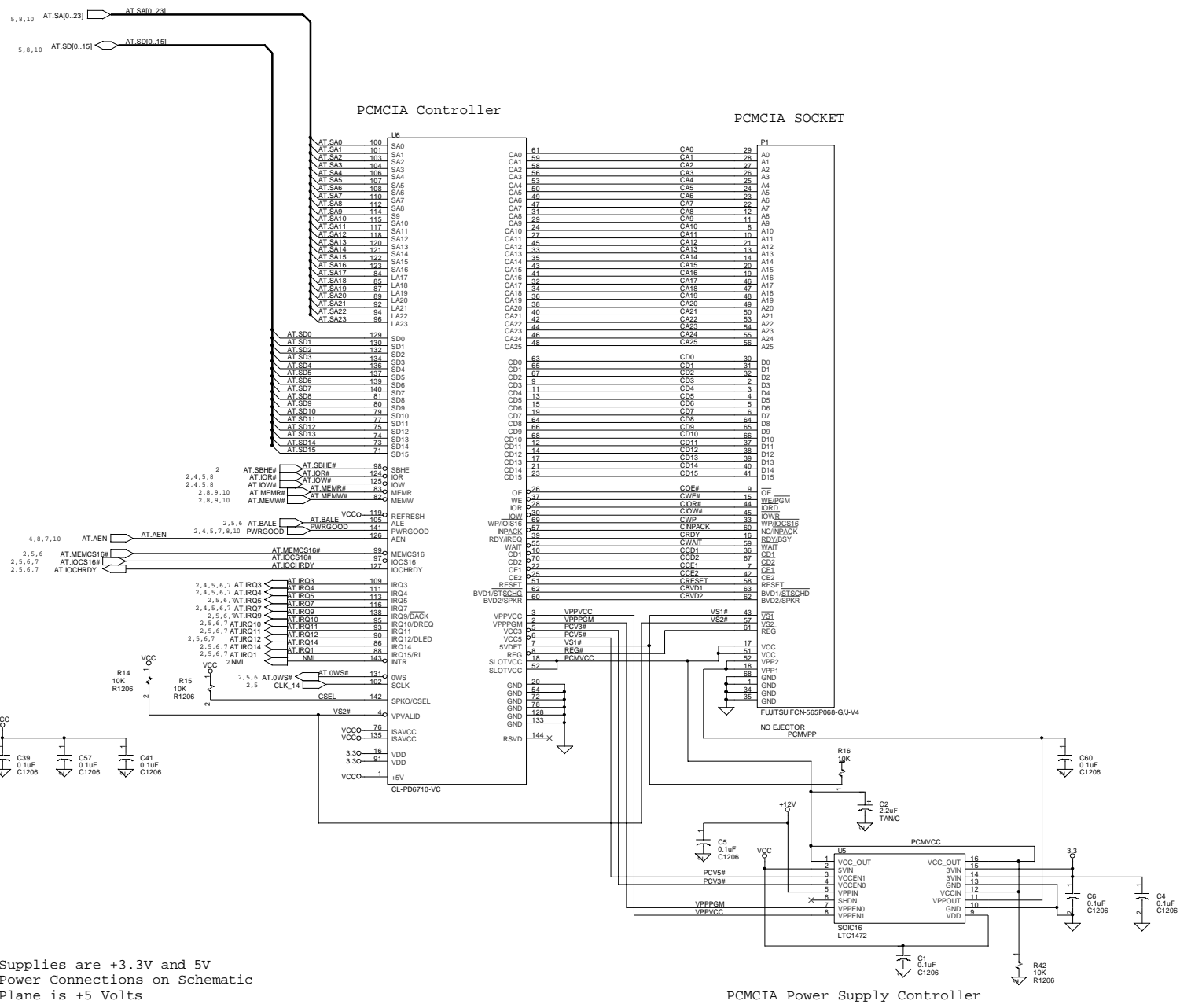
U27 Supply = VCC = +5V  
 VCC Plane is +5 Volts

Jumpers	Comment
1-3	Write to Flash except Boot Block
1-3 & 2-6	Write to Flash and Boot Block



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Title		
Sample Design BIOS Flash ROM Circuitry		
Size B	Document Number	Rev 1.0
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U21 Supplies are +3.3V and 5V  
 See Power Connections on Schematic  
 VCC Plane is +5 Volts

PCMCIA Power Supply Controller

