i960® RM/RN I/O Processor

Specification Update

January 1999

Notice: The 80960RM/RN may contain design defects or errors known as errata. Characterized errata that may cause 80960RM/RN's behavior to deviate from pubished specifications are documented in this specification update.

Order Number: 273164-003

Contents

Revision History

Date	Version	Description
01/20/99	003	Added the following Errata: #7, Data Corruption Occurs when Transfer Data Value Matches the Memory Mapped Register (MMR) Addresses of the DMA Channels. #8, Data Corruption Occurs when Transfer Data Value Matches the Memory Mapped Register (MMR) Addresses of the Application Accelerator Unit. Added the following Specification Changes: #1, Default Value of the Memory Controller's Refresh Frequency Register (RFR). #2, Resetting the Memory Controller's SDRAM Output Buffers during the Power-Fail Sequence. #3, PCI-to-PCI Bridge Configuration Registers: Bridge Subsystem Vendor ID Register (BSVIR) and Bridge Subsystem ID Register (BSIR). Added the following Documentation Change: #3, Section 12.3.1 of the i960® RM/RN I/O Processor Developer's Manual.
01/13/99	002	Added the following Specification Clarifications: #1, Hooking up the SDRAM Clock Enable Inputs on the SDRAM DIMM for Non- Battery-Backup Applications #2, Hooking up the SDRAM Clock Enable Outputs (SCKE0 and SCKE1) from the i960® RM/RN I/O Processor to the Clock Enable Inputs on the SDRAM DIMM in a Battery-Backup Application
8/98	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order #
i960® RM/RN I/O Processor Developer's Manual	273158
80960RM I/O Processor Data Sheet	273156
80960RN I/O Processor Data Sheet	273157
i960® RM/RN I/O Processor Design Guide	273139

Nomenclature

Errata are design defects or errors. These may cause the Product Name's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	Errata
	A-0	#	#			
1	X			11	NoFix	The ATU Discard Timer Status Bit in ATUCR Gets Set Even Though Delayed Read/Write Completes Before Discard Timer Expires
2	X			11	NoFix	A Target Abort Occurs on the Internal Bus when Target Abort Passing from the Internal Bus to the PCI Buses through the ATUs is Disabled
3	X			12	NoFix	After Initialization, Changing the Configuration Cycle Retry Bit in the EBCR to Retry Configuration Cycles while they are Occurring can Cause Data Corruption
4	X			12	NoFix	A Target Abort from the Internal Bus may be Reported to the PCI Bus, Without the Target Abort Being Returned
5	X			12	NoFix	Secondary Interrupts are Routed to the Core Processor, Rather than the Primary PCI Bus, as their Default
6	X			13	NoFix	Secondary IDSEL Select Register (SISR) Bits are in Reverse Order
7	X			13	Fix	Data Corruption Occurs when Transfer Data Value Matches the Memory Mapped Register (MMR) Addresses of the DMA Channels
8	X			15	Fix	Data Corruption Occurs when Transfer Data Value Matches the Memory Mapped Register (MMR) Addresses of the Application Accelerator Unit

Specification Changes

No.	Steppings			Page	Status	Specification Changes
	A-0	#	#			
1	X			16	Fix	Default Value of the Memory Controller's Refresh Frequency Register (RFR)
2	X			16	Fix	Resetting the Memory Controller's SDRAM Output Buffers during the Power-Fail Sequence
3	X			16	Fix	PCI-to-PCI Bridge Configuration Registers: Bridge Subsystem Vendor ID Register (BSVIR) and Bridge Subsystem ID Register (BSIR)

Specification Clarifications

No.	Steppings			Page	Status	Specification Clarifications
	A-0	#	#			
1	X			17	Doc	Hooking up the SDRAM Clock Enable Inputs on the SDRAM DIMM for Non- Battery-Backup Applications
2	X			17	Doc	Hooking up the SDRAM Clock Enable Outputs (SCKE0 and SCKE1) from the i960® RM/RN I/O Processor to the Clock Enable Inputs on the SDRAM DIMM in a Battery-Backup Application

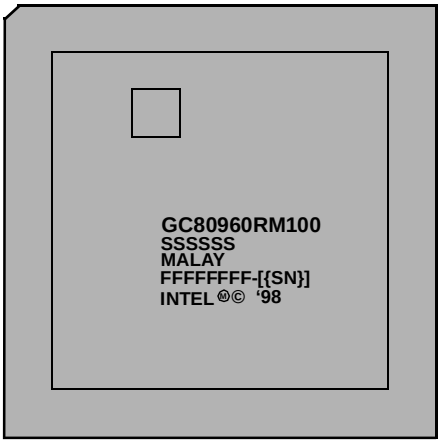
Documentation Changes

No.	Document Revision	Page	Status	Documentation Changes
1	273139-001	20	Doc	Page 1 of 80960RM Schematics and Page 1 of 80960RN Schematics
2	273139-001	21	Doc	Page 1 of 80960RM Schematics and Page 1 of 80960RN Schematics
3	273158-001	21	Doc	Section 12.3.1 of the i960® RM/RN I/O Processor Developer's Manual

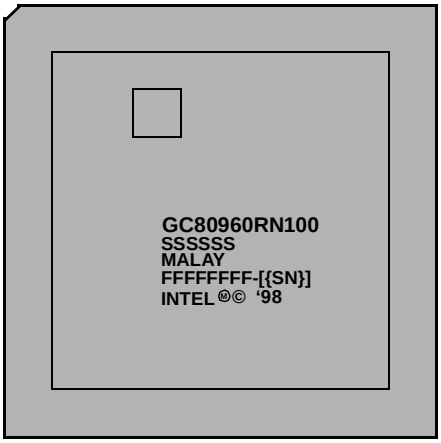
Identification Information

Markings

Topside Markings



80960RM



80960RN

Device ID Registers

Device and Stepping	Processor Device ID Register (PDIDR - 0x1710)	PCI-to-PCI Bridge Unit Revision ID (RIDR - 0x1008)	Address Translation Unit Revision ID Register (ATURID - 0x1208)	i960® Core Processor Device ID (DEVICEID - 0xFF00 8710)
80960RM A-0	08862013	0x0	0x0	00823013
80960RN A-0	08863013	0x0	0x0	00823013

Errata

1. The ATU Discard Timer Status Bit in ATUCR Gets Set Even Though Delayed Read/Write Completes Before Discard Timer Expires

Problem: The ATU Discard Timer Status bit (bit 15, in the Address Translation Unit Configuration Register, local bus address 1288H) is getting set even though the transaction completed correctly. This scenario occurs when a single-word delayed read or write is completing on the PCI bus through either the primary ATU or the secondary ATU at the same time that the discard timer is timing out. This should not affect multi-word transactions, but should occur with all configuration reads and writes that line up with the discard timer time-out.

Implication: Although the discard timer time-out bit is being set, the transaction is completing properly, so the only implication here is the handling of any actions that occur as a result of the discard timer being set.

Workaround: Software that handles the discard timer status bit, should just reset the ATU Discard Timer Status bit (bit 15, in the Address Translation Unit Configuration Register, local bus address 1288H) in this scenario. The likelihood of seeing the problem is reduced if the timer value is set to 2^{15}.

Status: NoFix. See the Table "Summary Table of Changes" on page 7.

2. A Target Abort Occurs on the Internal Bus when Target Abort Passing from the Internal Bus to the PCI Buses through the ATUs is Disabled

Problem: If a target abort occurs on the Internal Bus due to an ECC error, and target abort passing from the internal bus to the PCI busses is disabled, the ATU can deadlock when all the following conditions are true:

- The PCI master must be a 32-bit master
- The PCI master induces data-to-data wait states
- A target abort occurs on the internal bus
- The Primary (bit 0, in the Primary ATU Interrupt Mask Register, local bus address 12BCH) or Secondary (bit 0, in the Secondary ATU Interrupt Mask Register, local bus address 12C0H) ATU ECC Target Abort Enable bit is clear.

Implication: Under these conditions the relevant ATU will not pass the target abort back to the PCI master, and the ATU will enqueue subsequent read transactions, but will never return data. The discard timer will not rescue this case, since pointers have been corrupted.

Workaround: Always set The Primary ATU ECC Target Abort Enable bit (bit 0, in the Primary Interrupt Mask Register, local bus address 12BCH) and the Secondary ATU ECC Target Abort ENable bit (bit 0, in the Secondary Interrupt Mask Register, local bus address 12C0H) to allow the ATUs to pass the target abort back to the PCI master.

Status: NoFix. See the Table "Summary Table of Changes" on page 7.

3. After Initialization, Changing the Configuration Cycle Retry Bit in the EBCR to Retry Configuration Cycles while they are Occurring can Cause Data Corruption

Problem: After initialization, if the Configuration Cycle Retry Bit (bit 2, in the Extended Bridge Configuration Register, local bus address 1040H) is changed to retry configurations cycles at the same time that a configuration read completion is starting on the primary PCI bus, the ATU will return data, but will not dequeue it.

Implication: Under the above conditions, if another read of the same address were to occur, the old, stale data in the queue would be returned to the master.

Workaround: Do not change the Configuration Cycle Retry Bit (bit 2, in the Extended Bridge Configuration Register, local bus address 1040H) after initialization.

Status: NoFix. See the Table "Summary Table of Changes" on page 7.

4. A Target Abort from the Internal Bus may be Reported to the PCI Bus, Without the Target Abort Being Returned

Problem: If a target abort occurs on the internal bus before the 'primary' Memory Enable Bit (bit 1, in the Primary ATU Command Register, local bus address 1204H) is cleared, or the 'secondary' Memory Enable Bit (bit 1, in the Secondary ATU Command Register, local bus address 1298H) is cleared, the target abort will be reported incorrectly in the ATU error registers, when the transaction master aborts on the relevant PCI bus. Furthermore, the transaction will be dequeued.

Implication: If the memory enables are turned back on, the original target abort will be lost. Also, if enabled, this WILL generate an interrupt to the core.

Workaround: Ensure that the queues in the ATUs are cleared before changing the Memory Enable Bit (bit 1, in the Primary ATU Command Register, local bus address 1204H) or the Memory Enable Bit (bit 1, in the Secondary ATU Command Register, local bus address 1298H) after initialization.

Status: NoFix. See the Table "Summary Table of Changes" on page 7.

5. Secondary Interrupts are Routed to the Core Processor, Rather than the Primary PCI Bus, as their Default

Problem: The secondary interrupts (S_INTA#, S_INTB#, S_INTC#, and S_INTD#) are routed to the 80960RM/RN core processor as their default. They should be routed to the primary PCI bus as their default.

Implication: When booting in configuration mode 0, cards located on the secondary PCI bus will have their interrupts routed to the i960 core processor and may not function correctly in the system.

Workaround: Boot the processor in Mode 3 (Default Mode), and set the S_INTA# Select Bit, S_INTB# Select Bit, S_INTC# Select Bit, and S_INTD# Select Bit (Bits 3:0, in the PCI Interrupt Routing Select Register, local bus address 1050H) in the initialization software. Then make sure to clear the Configuration Cycle Retry Bit (bit 2, in the Extended Bridge Control Register, local bus address 1040H) to allow the bridge and the ATU to accept configuration cycles. If the system must boot in mode 0, these bits can be modified by an external agent on the PCI bus by using PCI configuration cycles.

Status: NoFix. See the Table "Summary Table of Changes" on page 7.

6. Secondary IDSEL Select Register (SISR) Bits are in Reverse Order

Problem: The bits in the Secondary IDSEL Select Register (SISR) are in reverse order Refer to Table 1 “SISR Bit Mapping” on page 13 for the bit descriptions.

Table 1. SISR Bit Mapping

Bit Number	Description
Bit 09	AD16 IDSEL Disable
Bit 08	AD17 IDSEL Disable
Bit 07	AD18 IDSEL Disable
Bit 06	AD19 IDSEL Disable
Bit 05	AD20 IDSEL Disable
Bit 04	AD21 IDSEL Disable
Bit 03	AD22 IDSEL Disable
Bit 02	AD23 IDSEL Disable
Bit 01	AD24 IDSEL Disable
Bit 00	AD25 IDSEL Disable

Implication: When private devices are being used on the secondary side and the SISR is programmed without taking the bit reversal into account, the private devices may not be hidden from the host. In addition, public devices may be hidden from the host.

Workaround: Program the SISR with the new bit mapping as described above.

Status: NoFix. See the Table “Summary Table of Changes” on page 7.

7. Data Corruption Occurs when Transfer Data Value Matches the Memory Mapped Register (MMR) Addresses of the DMA Channels

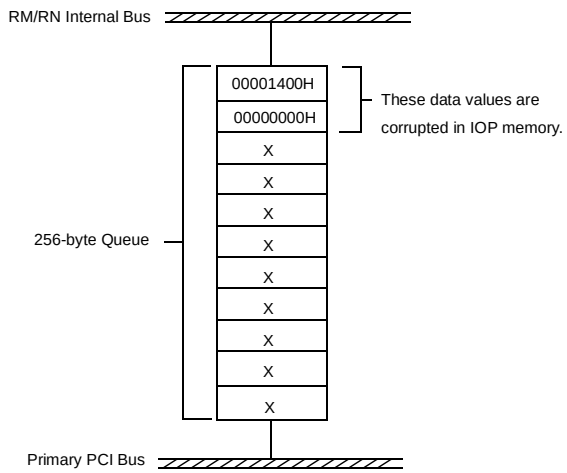
Problem: This problem appears across all 3 DMA channels: DMA Ch-0, Ch-1, and Ch-2. If the transfer data value falls within the MMR address range of the active DMA channel (1400H - 143FH for Ch-0, 1440H - 147FH for Ch-1, and 1480H - 14FFH for Ch-2), data corruption will occur.

Examples on page 14 describe the error condition.

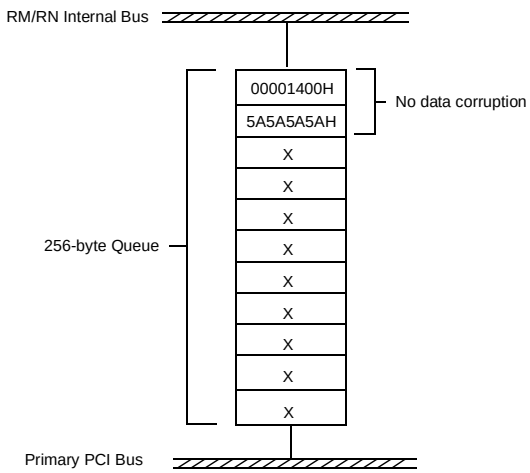
Assumption: DMA channel 0 is used to transfer data from PCI to IOP memory.

Single Transaction on the Internal Bus

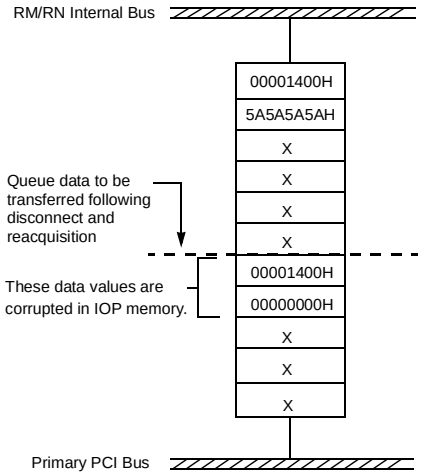
Case 1



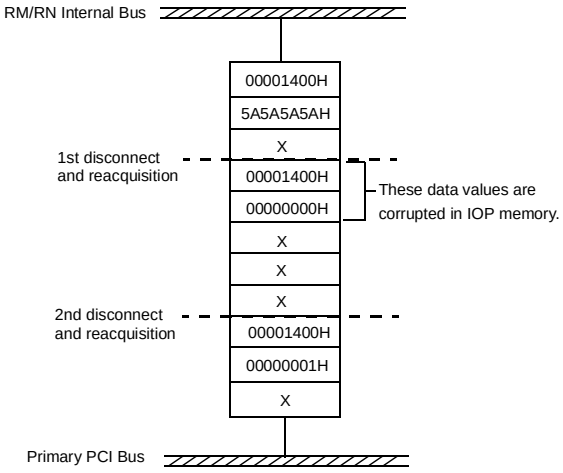
Case 2



Case 3: Two Transactions on the Internal Bus (one disconnect)



Case 4: Three Transactions on the Internal Bus (two disconnects)



Implication: Data corruption results when the data value matches the MMR address range of the active DMA channel.

Workaround: There are two possible workarounds for this errata:

- Use the Primary Address Translation Unit (PATU) to transfer data from Primary PCI to IOP memory and Secondary Address Translation Unit (SATU) to transfer data from Secondary PCI to IOP memory.
- Configure the Memory Controller Unit to execute in 32-bit mode. For further information, refer to Section 13.3.3 on page 13-14 of the *i960® RM/RN I/O Processor Developer's Manual* and to Table 4 in the 80960RM/RN I/O processor datasheets.

Status: Fix. A fix for this errata is planned for the B-0 stepping.

8. Data Corruption Occurs when Transfer Data Value Matches the Memory Mapped Register (MMR) Addresses of the Application Accelerator Unit

Problem: If the transfer data value falls within the MMR address range of the Application Accelerator Unit (1800H - 18FFH), data corruption will occur.

Implication: Data corruption results when the data value matches the MMR address range of the Application Accelerator Unit.

Workaround: There are two possible workarounds for this errata:

- Compute the XOR Parity calculation through software by using the i960® JT processor.
- Configure the Memory Controller Unit to execute in 32-bit mode. For further information, refer to Section 13.3.3 on page 13-14 of the *i960® RM/RN I/O Processor Developer's Manual* and to Table 4 in the 80960RM/RN I/O processor datasheets.

Status: Fix. A fix for this errata is planned for the B-0 stepping.

Specification Changes

1. Default Value of the Memory Controller's Refresh Frequency Register (RFR)

Issue: The Refresh Frequency Register (RFR) will default to the value 00H. The desired value of the RFR will need to be specified during the SDRAM initialization sequence/routine.

Status: Fix. This change is planned for the B-0 stepping.

2. Resetting the Memory Controller's SDRAM Output Buffers during the Power-Fail Sequence

Issue: SDRAM output buffers will be reset to the default value (low-drive strength) after the power-fail sequence has executed with the current buffer strength configuration.

Status: Fix. This change is planned for the B-0 stepping.

3. PCI-to-PCI Bridge Configuration Registers: Bridge Subsystem Vendor ID Register (BSVIR) and Bridge Subsystem ID Register (BSIR)

Issue: To guarantee compliance with the PCI-to-PCI Bridge Architecture Specification Rev 1.0, the Bridge Subsystem Vendor ID Register (BSVIR@PCI configuration offset 34H) and the Bridge Subsystem ID Register (BSIR@PCI configuration offset 36H) will be specified to be reserved in the configuration address space. Configuration software should therefore not write to these reserved locations.

Status: Fix. This change is planned for the B-0 stepping.

Specification Clarifications

1. Hooking up the SDRAM Clock Enable Inputs on the SDRAM DIMM for Non-Battery-Backup Applications

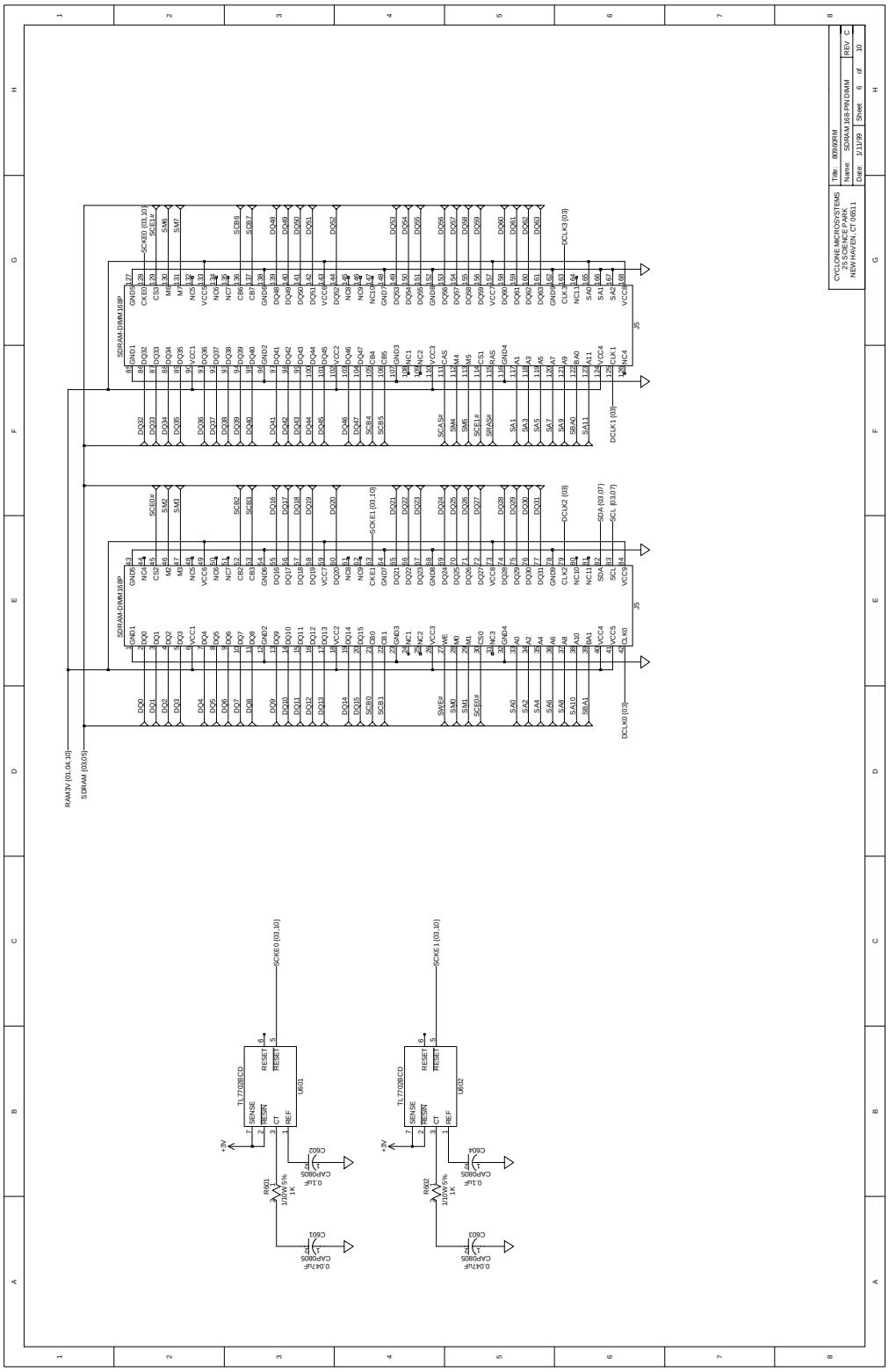
Problem: During the power-up reset sequence, the SDRAM devices occasionally enter a pseudo, self-refresh mode. This causes a lock-up condition on the SDRAM device. Normal operation of the SDRAM device which includes the SDRAM initialization sequence does not clear the lock-up condition.

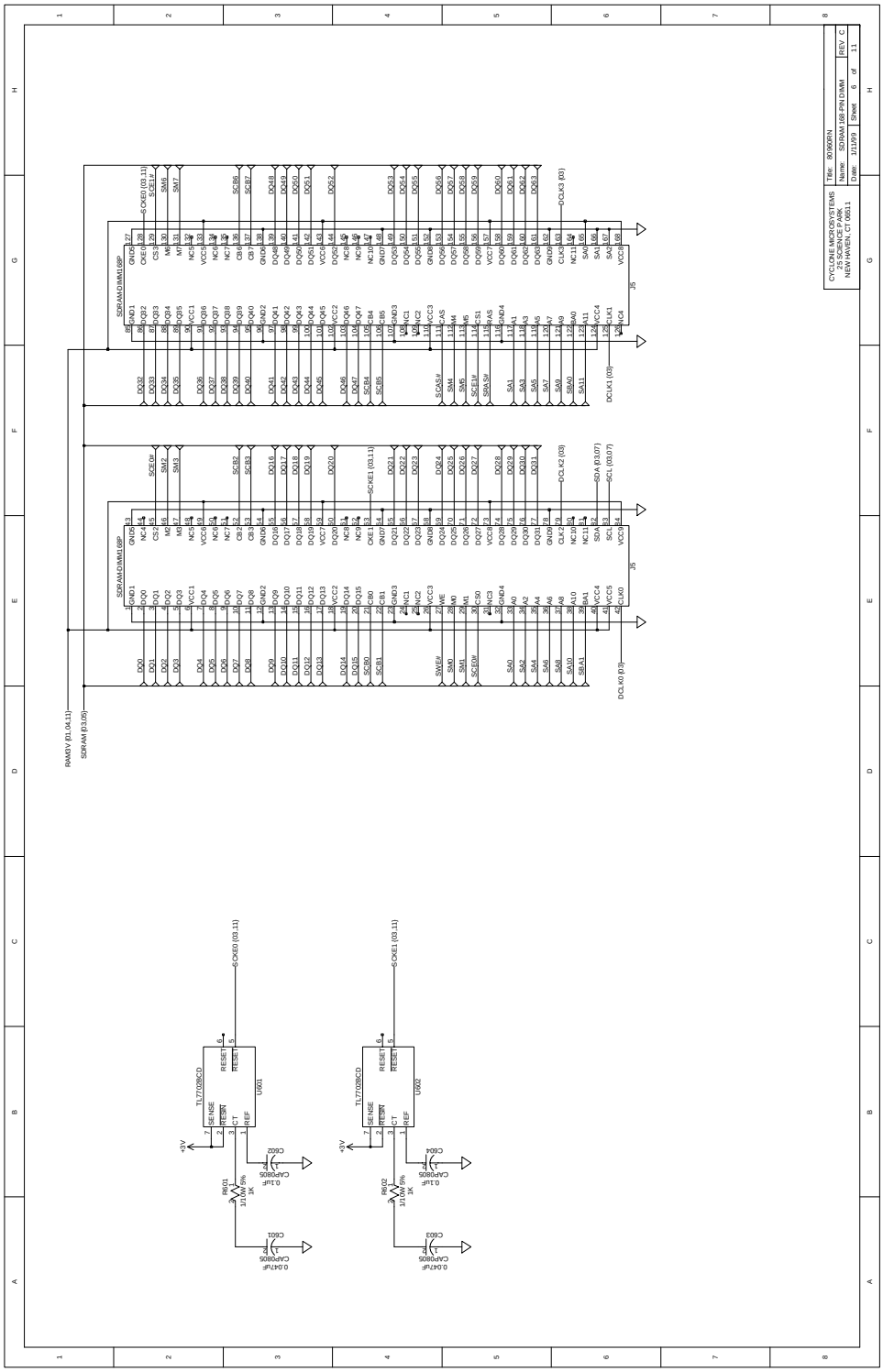
Workaround: Tie the Clock Enable Inputs on the SDRAM DIMM to V_{CC}.

2. Hooking up the SDRAM Clock Enable Outputs (SCKE0 and SCKE1) from the i960® RM/RN I/O Processor to the Clock Enable Inputs on the SDRAM DIMM in a Battery-Backup Application

Problem: During the power-up reset sequence, the SDRAM devices occasionally enter a pseudo, self-refresh mode. This causes a lock-up condition on the SDRAM device. Normal operation of the SDRAM device which includes the SDRAM initialization sequence does not clear the lock-up condition.

Workaround: Ensure that the Clock Enable Inputs to the SDRAM DIMM are held low during power-up. This is accomplished as shown in the following circuit schematics (Sheet 6 – 80960RM schematics and Sheet 6 – 80960RN schematics in *i960® RM/RN I/O Processor Design Guide*).

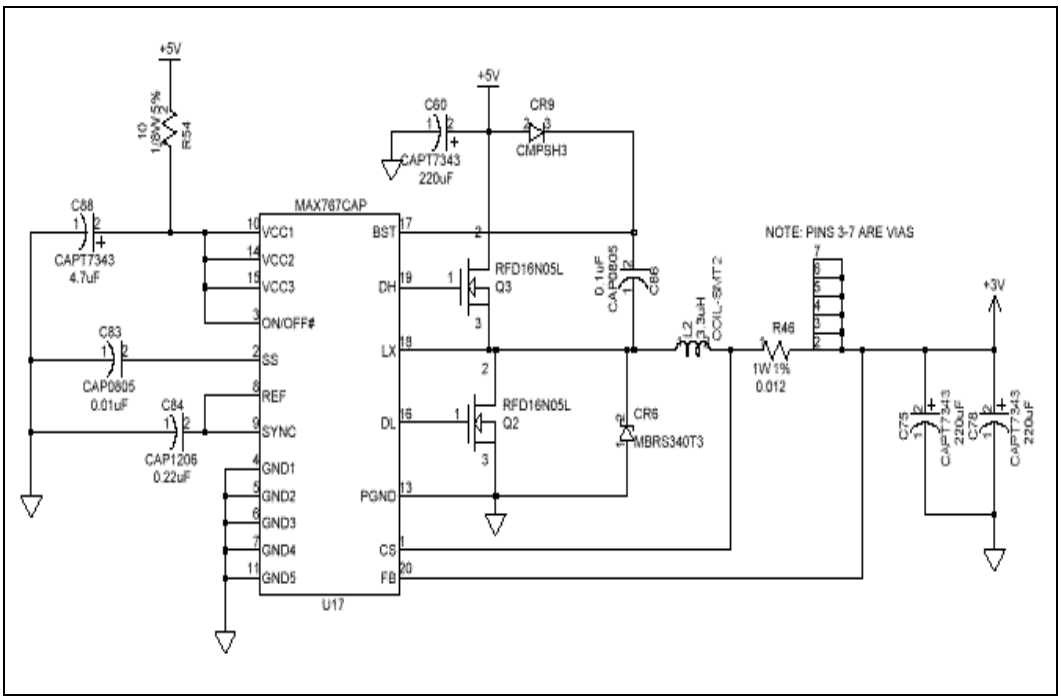




Documentation Changes

1. Page 1 of 80960RM Schematics and Page 1 of 80960RN Schematics

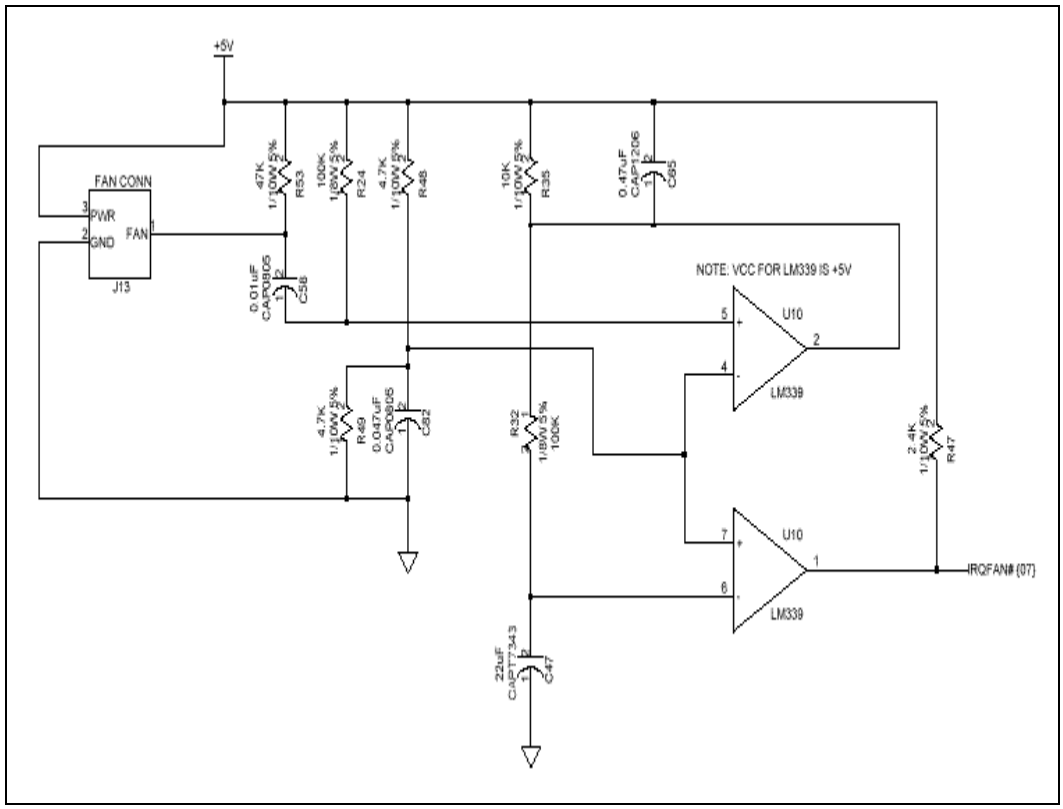
Issue: FETs Q2 and Q3 have had pinout changes as shown below.



Affected Docs: *i960® RM/RN I/O Processor Design Guide*.

2. Page 1 of 80960RM Schematics and Page 1 of 80960RN Schematics

Issue: The fan connector, J13, has been changed by the manufacturer as shown below.



Affected Docs: *i960® RM/RN I/O Processor Design Guide.*

3. Section 12.3.1 of the i960® RM/RN I/O Processor Developer's Manual

Issue: The last sentence of the third paragraph has been modified as follows:

- Old:
  Logical Memory Mask register (LMMSK).
- New:
  Logical Memory Mask register (LMMR).

Affected Docs: *i960® RM/RN I/O Processor Developer's Manual.*