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APPLICATION BRIEF

Upgrade Path from 8096-90 to 8096BH to 80C196

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Converting applications that use an 8X9X-90 to use an 8X9XBH requires consideration of a few of the BH enhancements. Descriptions of each of the differences between the -90 and the BH follow, along with a discussion of the implications of the change.

$\overline{BHE}$ and INST are latched: The bus control signals $\overline{BHE}$ and INST are valid throughout the bus cycle on 8X9XBH devices. ON -90 devices, these signals need to be latched on the falling edge of ALE.

Byte Read following $\overline{RESET}$ rising: The bus control and buswidth options of 8X9XBH devices are selected by configuration of the chip immediately following the rising edge of $\overline{RESET}$. During the usual 10 state reset sequence, BH parts will perform a byte read of location 2018H to acquire configuration information prior to fetching the first opcode at location 2080H. The 8X9X-90 does not perform this read.

ALE is high while in reset: The ALE/$\overline{ADV}$ pin of the 8X9XBH is driven high while the $\overline{RESET}$ pin is held low. On -90 devices, ALE is driven low while in RESET. Circuits which rely on the state of ALE while RESET is low must be modified. The reset state of ALE was changed to enable implementation of the Chip Configuration Byte read from external memory following the rising edge of RESET.

$\overline{EA}$ is latched on $\overline{RESET}$ rising: The 8X9XBH latches the value of $\overline{EA}$ on the rising edge of $\overline{RESET}$. On -90 devices, $\overline{EA}$ was not latched and could be changed without placing the part in $\overline{RESET}$. This change was necessary to enhance ROM/EPROM security. Circuits that rely on $\overline{EA}$ not being latched must be modified.

A/D speed increased: The 8X95BH and 8X97BH A/D converters complete conversion in 88 state times. On -90 devices with A/D converters, a conversion takes 168 state times. This translates in an increased conversion speed from 42μs on -90 parts to 22μs on BH parts running at 12MHz. Software that relies upon the speed of conversion for timing must be changed. It is also recommended that MCS-96 software be written so as to not be impacted by further changes in A/D conversion speed.

Sample/Hold on A/D: The 8X95BH and 8X97BH have a sample/hold on the input of the A/D converter. 8X9X-90 devices with A/D converters do not have sample/hold circuitry. External analog circuitry which also includes a sample/hold must provide a settled analog input within the first four state times of 8X9XBH conversion.

Duplicate Fetches: The 8X9XBH bus controller was made more aggressive when it comes to instruction fetches in order to minimize the execution speed degradation of using an 8-bit bus. As a result, instruction fetches over a 16-bit bus sometimes occur when there is no space in the prefetch queue to store the fetched opcodes. This requires another instruction fetch from the same address when space in the prefetch queue opens up.

To the external system, these occurrences appear as duplicate instruction fetches. An estimated 10 percent of all instruction fetches will be "duplicates", while overall bus loading will be approximately 65 to 70 percent, compared to an 8X9X-90 bus loading of approximately 55 to 60 percent. Execution speed is not impacted by a duplicate fetch.

Write Pulse Width: The 8X9XBH 16-bit bus write pulse width is one T_{osc} longer than on the 8X9X-90, thus allowing slower memories and peripherals to be used. In order to widen the $\overline{WR}$ pulse width, the time between the end of $\overline{WR}$ and the next ALE was reduced by T_{osc}. Note that the signals $\overline{WRL}$, $\overline{WRH}$, and $\overline{WR}$ with an 8-bit bus are still the same width as on -90 parts.

V_{PP} Replaces V_{BB}: V_{PP} is the programming pin for EPROM devices. Systems that have this connected through a capacitor to ANGND (required on 8X9X-90 parts) do not need to change. ANGND must be held nominally at the same potential as V_{SS}, and V_{PP} must NOT be connected to V_{CC}. High voltage must NEVER be placed on the V_{PP} pin of a ROM device.

While there is almost no reason to do so, an application should not attempt to execute with the EA pin at logic zero and V_{CC} at 5.5 V_{DC} on an 879XBH EPROM device. Additionally, the design should always begin the "out of RESET" code execution from the internal EPROM, immediately after the power-on sequence.

Reserved location warning: Intel reserved addresses can not be used by applications which use 8X9XBH internal ROM/EPROM. The data read from a reserved location is not guaranteed, and a write to any reserved location could cause unpredictable results. When attempting to program Intel Reserved addresses, the data must be OFFFFH to ensure a harmless result.

Intel Reserved locations, when mapped to external memory, must be filled with OFFFFH to ensure compatibility with future parts.

A positive transition on NMI: The 8X9XBH does not clear the Watchdog Timer. The 8X9X-90 does clear the WDT on a positive transition of NMI, and both part vector to external address 0000H.

The following is the latest information on upgrading a NMOS 8096 to a CHMOS 80C196.

The chip which is the CHMOS 8096BH replacement is designated the 80C196. The part can be configured to be pin compatible with the 8096, but because of the process change and other enhancements, it may not be plug compatible in some designs. This is to say that you will not be able to arbitrarily swap out a NMOS 8096 and replace it with the 80C196. However, if a few rules are followed the changes required will be almost painless.

80C196 OVERVIEW

First, some background on the 80C196 is needed. The opcode set is a true superset of the 8096, but some enhancements have been made to the peripherals and timings. The crystal is divided by 2 on the 80C196, instead of 3, as on the 8096. This means that the 80C196 running at 8 MHz will have a 250 ns state time, Just like an 8096 running at 12 MHz.

An 80C196 running at 8 MHz will emulate an 8096 at 12 MHz except that some of the instructions and peripherals will operate faster. The instructions which will be speeded up include mul, div, interrupt, call, ret, and jumps. The serial port will require a different baud value and the A to D may not run at exactly the same speed. This means that timing loops which measure instruction speed or A to D completion speed may have to be modified. The bus timings, while not nanosecond for nanosecond compatible, will work in most systems.

DESIGN GUIDELINES

1. Do not use undefined register areas for storage or depend on them to return a specific value if it is not stated in the Embedded Controller. Undefined registers and locations on this, or any other, part should be considered off-limits and reserved for development systems, testing or future use.
2. Do not base timings loops on instruction execution times, as some instructions may execute faster on the 80C196 than on the 8096, even when the 80C196 is slowed down to 8 MHz, its 8096 compatible rate. Counter-type loops should be initialized with values that can easily be changed at compile time.
3. Do not base critical timings on interrupt responses, A to D completions, flag settings, etc. This is for the same reason as above; some of these responses may be slightly different from those on the 8096. Timer 1 is provided for critical timings. With an 8 MHz crystal, it will increment every 2 microseconds, just as an 8096 running at 12 MHz.
4. The serial port baud register values should be easily changeable at compile time. Since the serial port is now capable of running at a higher frequency, a different baud rate value will be needed.
5. The circuitry interfacing to the chip should be capable of interfacing to the 80C196. The I/O lines on 80C196 will look a lot like those on the 80C51.
6. The $\overline{BHE}/\overline{WRH}$ signal in eight bit and write strobe mode will go low for odd byte transfers and high for even byte transfers. The $\overline{WR}/\overline{WRL}$ signal will go low for odd byte transfers and high for even byte transfers. Normally, the $\overline{WR}/\overline{WRL}$ signal should go low for odd and even byte transfers since transfers are on the low byte of the data bus.
7. PUSH and POP operations addressed relative to the stack pointer work differently on the 80C196 than on the 8096. On the 8096, the address is calculated based on the un-updated stack pointer value, on the 80C196, the address is calculated based on the updated value. The only operations effected are: PUSH xx[sp], PUSH [sp], PUSH sp, POP xx[sp], POP [sp], POP sp.
8. The V_{PD} pin on the 8X9X parts is now the CDE (Clock Detect Enable) pin on the 80C196. When tied high, CDE enables a clock speed sensor and will reset the part if the Xtal1 frequency drops below a few hundred KHz. While this is perfect for most production boards, it may be desirable to have a jumper option on this function for evaluation boards.

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