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# iSBC™ 550
ETHERNET™ COMMUNICATIONS CONTROLLER

- **Meets the version 1.0 tri-corporate Ethernet specification**
- **Ethernet data link layer support**
  - **Data encapsulation**
  - **Framing and packet control**
  - **Buffer management**
- **Ethernet physical link layer support**
  - **Serial/deserialization**
  - **10 Mbits per second data rate**
  - **CRC generation/check**
  - **Carrier-sense multiple-access with collision detection (CSMA/CD)**
  - **Transceiver interface compatibility**

- **Easy-to-use MULTIBUS® inter-processor protocol supported in firmware**
- **Power-up confidence test assures integrity of on-board memory and programmable LSI**
- **Traffic, errors and collision information maintained for network management**
- **Excellent foundation for Ethernet local area end-to-end network**

The iSBC 550 Ethernet Communications Controller meets the tri-corporate (DEC, Xerox, Intel) specification for Ethernet local area networks. All the functions of the Ethernet data link layer and physical link layer are provided on two 6.75 x 12″ circuits boards and associated firmware. The MULTIBUS compatible controller can be utilized as the foundation for a single board computer (iSBC)-based Ethernet local area network or as a prototype for Intel® 8085, iAPX™ 88, or iAPX 86 component-based Ethernet applications. The iSBC 550 controller's firmware (supplying the Ethernet and system interface) has an easy-to-use MULTIBUS Interprocessor Protocol (MIP) facility, which is readily accessed from another iSBC Board using a custom run-time software system or Intel's iRMX™ 80/88/86 Real-Time Executive software and the iMMX™ 800 (MULTIBUS Message Exchange) software package. The Ethernet data link functions are divided between the processor board which provides the data link layer's software to control the data encapsulation and the link management, and the serial/deserialization (SerDes) board which provides the 10-MBit per second serial interface to the Ethernet transceiver.
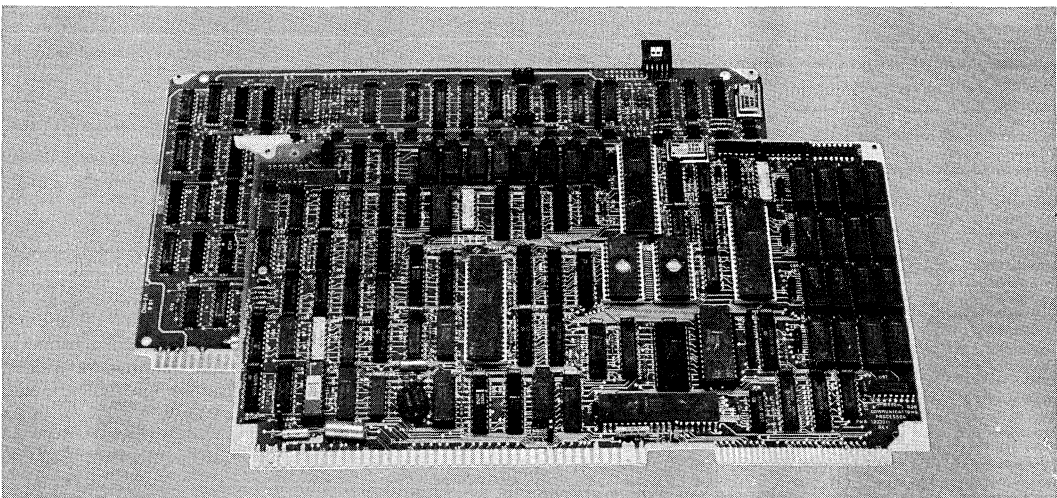
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FUNCTIONAL DESCRIPTION

The iSBC 550 Ethernet Communications Controller is a two-board MULTIBUS-compatible set that offers high-speed Ethernet-compatible data transfer between digital devices operating at a 10-Mbit per sec data rate. The iSBC 550 controller can effectively support the needs of local area network applications, such as office automation, distributed data processing, factory data collection, research data collection, intelligent terminal and other EDP-related products.

Ethernet Specification

The Ethernet network is a local area network concept that is jointly being supported by Intel Corporation, Digital Equipment Corporation, and Xerox Corporation. The network is designed to link systems over a distance of up to 2500 meters using an available 50-ohm coaxial cable. Several hundred stations may be connected to the cable which supports a data rate of 10 Megabits per second. The data is encapsulated in a packet message format. The data signal is a base-band, Manchester-encoded type that is self-synchronizing.

The jointly developed Ethernet specification, "The Ethernet, A Local Area Network Data Link Layer and Physical Link Layer Specification, Version 1.0, September 30, 1980", precisely defines the two lower layers of a local area network architecture where the system is a series of independent layers. The lowest layer, the physical link layer, is concerned with coaxial cable interface. The data link layer supports the peer protocol's statistical contention resolution (CSMA/CD) and link management functions. All additional network layers are defined by the user during the implementation of the application-specific layers.

Ethernet Data Link Layer Support

The iSBC 550 processor board provides the data link layer's software to control the data encapsulation and the link management, including frame delimitation, address handling, error detection, and collision handling. After the iSBC 550 processor board is initialized upon system start-up or reset, the data link firmware is ready to service the local area network commands. An example of a command structure sent the iSBC controller to receive a packet of data from the Ethernet link is shown in Figure 1. The message passed via the MIP (MULTIBUS Interprocessor Protocol) interface is composed of two parts, the iSBC 550 controller information (including the command and associated data), and the required Ethernet information.
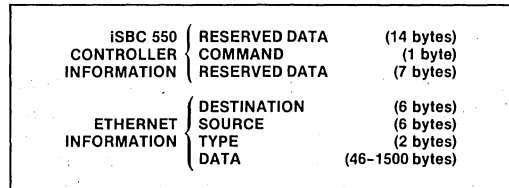
```
   iSBC 550  ┌ RESERVED DATA      (14 bytes)
 CONTROLLER  ┤ COMMAND             (1 byte)
INFORMATION  └ RESERVED DATA       (7 bytes)

             ┌ DESTINATION         (6 bytes)
   ETHERNET  ┤ SOURCE              (6 bytes)
INFORMATION  │ TYPE                (2 bytes)
             └ DATA         (46–1500 bytes)
```

Figure 1. Data Link for SUPPLYBUF Command Format

Shown in Table 1 are eight external Ethernet controller commands available to a user's application via the MIP interface. The commands manage the Ethernet multicast address recognition, message type connection, message flow, and overall network statistics.

Table 1. External Controller Commands

Command	Function
CONNECT	Indicates the data link message TYPE to be *connected* to user program.
DISCONNECT	*Disconnects* the data link TYPE from the user's application.
ADDMCID	*Adds* a multicast ID for recognition.
DELETEMCID	*Delete* the specified multicast ID.
TRANSMIT	*Transmit* a data packet to the Ethernet link.
SUPPLYBUF	*Supplies* a buffer for packet reception from the Ethernet link ("receive" function).
READ	*Read* the statistical variables maintained by data link layer.
READC	*Read* and *clear* the statistical variables.

Ethernet Physical Link Layer Support

The Serialization/Deserialization (SerDes) board provides the required electrical characteristics of the physical link layer of the Ethernet architecture for a transceiver interface. The transceiver is a device physically attached to the coax cable which does signal conditioning for transmitting and receiving.

Many major functions are controlled by the SerDes board. These functions include serialization/deserialization, packet framing, Manchester encoding/decoding, transmit data flow control, receive data flow control, destination address decoding for received message, CRC generation and

checking, and diagnostics for CRC error, loop-back, transmit timeout, and CSMA/CD (Carrier-Sense Multiple-Access with Collision-Detection).

Easy-To-Use Interface

One of the iSBC 550 controller boards is an iAPX 88-based processor board which has firmware support for the user's application interface. The programmatic interface utilizes the MULTIBUS Interprocessor Protocol (MIP) interface to the processor board. This interface is concerned with the message-passing protocol between multiple-processors. The iMMX 800 (MULTIBUS Message Exchange) software supports the MIP interface and offers a convenient quick-start method for users of Intel's iRMX 80, iRMX 88 executives and iRMX 86 operating system products for an Ethernet-based application.

Confidence Test

An effective diagnostic function is implemented in firmware on the processor board. This function is invoked at system initialization during both power-up and system reset time. These functions include: packet CRC checking, memory test, controller loopback, and other error tests. The tests provide a fundamental level of controller integrity.

Network Statistics

Statistics maintained by the data link firmware include packet traffic counts, collision information and error totals. This information can be effectively utilized by the user's application to understand the network's operation.

End-To-End Networking Foundation

The iSBC 550 controller provides the foundation data link layer and the physical link layer for a local area network architecture. Typically, the higher levels are user-defined and include the transport and the session control layers. The transport control layer is concerned with the end-to-end communications and the virtual channel connection via a port-to-port address. The session control layer provides the process-to-process control function which includes symbolic name binding and the establishment of the virtual connection via the transport control layer. In addition, the session control provides the specific error and recovery control responsible for message delivery.

The higher levels of the local area network architecture (see Figure 2) which use the data link layer are outside of the Ethernet standard, but can be implemented quickly on companion iSBC boards (e.g., iSBC 80/24, iSBC 88/25, iSBC 86/12A) running under the iRMX 80/88/86 Real-Time Multitasking Executives, respectively, and associated iMMX MULTIBUS Message Exchange (iMMX 800) software. Special iSBC 550 device driver software compatible with the iRMX 86 and iRMX 88 file systems is provided in the iMMX 800 package.
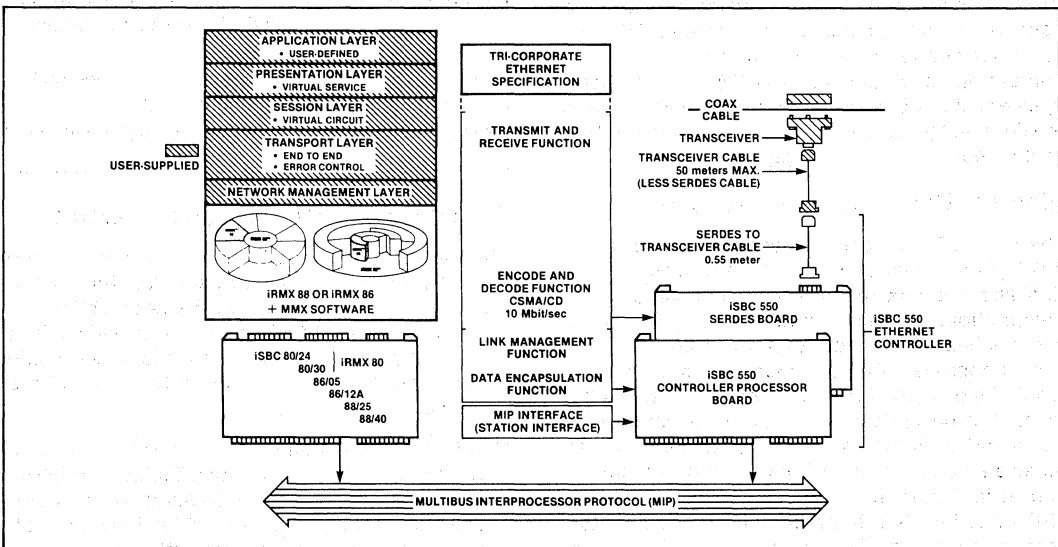

Figure 2. Ethernet Architecture and Implementation

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SPECIFICATIONS

Memory Addressing Capability

MULTIBUS System Bus — (00000–EFFFF)

Ethernet I/O Channels

One Ethernet electrically-compatible transceiver line on the SerDes board.

Interface Specifications

MULTIBUS System Bus — All signals TTL compatible.

Transceiver — All signals Ethernet specifications transceiver compatible.

Serial Communications Characteristics

Bit Serial Frame — Provides 64-bit *preamble*, 48-bit *destination* address, 48-bit *source* address, 16-bit *type*, 46–1500 bytes for *data*, and a *frame* check sequence of 32 bits.

Ethernet Network Specifications Supported

Coax Cable Length — 500-meter max.
Transceiver Cable Length — 50-meter max.
Number of Stations — 100 max.
Baud Rate — 10-Mbit/sec

System Clock

5.00 MHz, ± 0.1%

Physical Characteristics (Both Boards)

Width — 12.00 in. (30.48 cm) (each board)
Height — 6.75 in. (17.15 cm) (each board)
Depth — 0.5 in. (1.27 cm) (each board)
Weight — 3.5 lb (1.6 kg) (both boards)

SerDes to Transceiver Cable

Length — 0.55 meter (22 in.). Four pair twisted-wire cable with SerDes connector and transceiver interface connector.

Electrical Characteristics

Power requirements for both boards
+ 5 VDC @ 9.0A max.
+ 12 VDC @ 0.5A max.

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Relative Humidity — To 90% (without condensation)

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
MULTIBUS System	86	0.156	Viking 2KH43/9AMK12
SerDes Edge Connector	10	0.1	AMP 87631-5 Housing AMP 87195-9 Pins
Transceiver	15	0.1	Cinch Type DA 51220-1

Reference Manuals

121746 — iSBC 550 Ethernet Communications Controller Hardware Reference Manual (NOT SUPPLIED)

121769 — The Ethernet Communications Controller Programmer's Reference Manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

ORDERING INFORMATION

Part Number   Description

SBC 550   Ethernet Communications Controller for 10 Mbit/sec coaxial transmission. Includes Ethernet data link control software and cable to transceiver.