



8008/8008-1 8-BIT MICROPROCESSOR

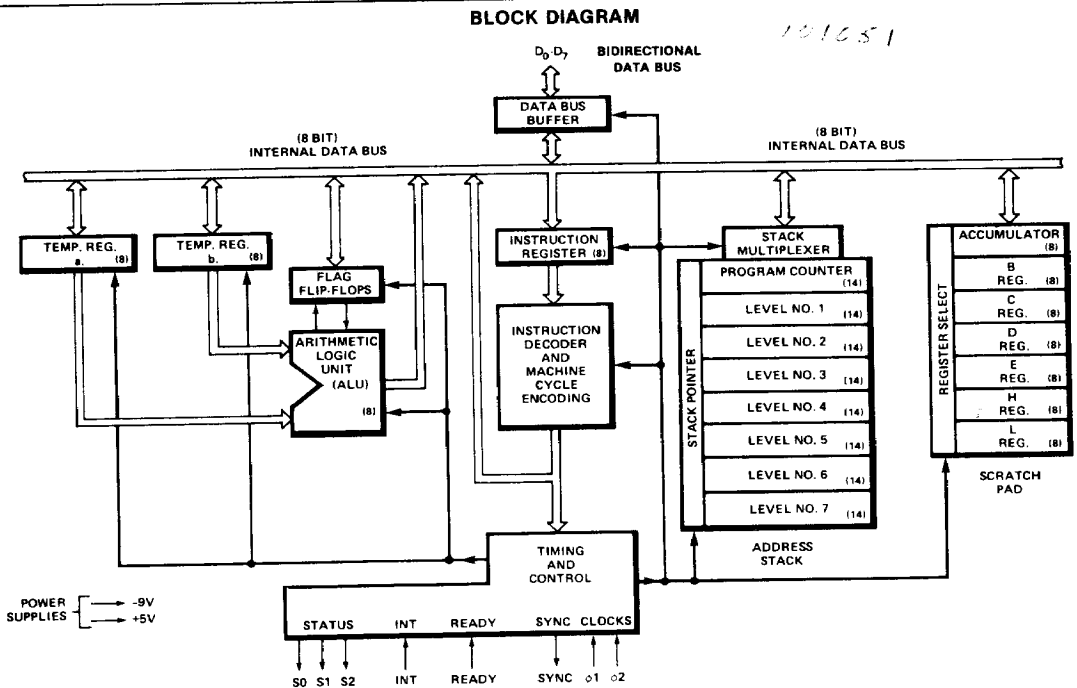
- Instruction Cycle Time — 1.25 μ s with 8008-1 or 20 μ s with 8008
- Directly Addresses 16K x 8 Bits of Memory (RAM, ROM, or S.R.)
- Interrupt Capability
- 48 Instructions, Data Oriented
- Address Stack Contains 8 14-Bit Registers (Including Program Counter) Which Permit Nesting of Subroutines Up to 7 Levels

The Intel® 8008 is a single chip MOS 8-bit parallel central processor unit (CPU) for the MCS-8 microcomputer system. This CPU contains 6 8-bit data registers, an 8-bit accumulator, 2 8-bit temporary registers, 4 flag bits (carry, zero, sign, parity), and an 8-bit parallel binary arithmetic unit which implements addition, subtraction, and logical operations. A memory stack containing a 14-bit program counter and 7 14-bit words is used internally to store program and subroutine addresses. The 14-bit address permits the direct addressing of 16K words of memory (any mix of RAM, ROM, or S.R.).

The instruction set of the 8008 consists of 48 instructions including data manipulation, binary arithmetic, and jump to subroutine.

The normal program flow of the 8008 may be interrupted through the use of the interrupt control line. This allows the servicing of slow I/O peripheral devices while also executing the main program.

The ready command line synchronizes the 8008 to the memory cycle allowing any type or speed of semiconductor memory to be used.



MCS-80/85

PIN DESCRIPTION

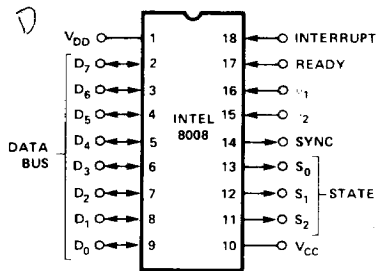


Figure 1. Pin Configuration

 D_0 - D_7

BI-DIRECTIONAL DATA BUS. All address and data communication between the processor and the program memory, data memory, and I/O devices occurs on these 8 lines. Cycle control information is also available.

INT

INTERRUPT input. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.

READY

READY input. This command line is used to synchronize the 8008 to the memory cycle allowing any speed memory to be used.

SYNC

SYNC output. Synchronization signal generated by the processor. It indicates the beginning of a machine cycle.

 ϕ_1, ϕ_2

Two phase clock inputs.

 S_0, S_1, S_2

MACHINE STATE OUTPUTS. The processor controls the use of the data bus and determines whether it will be sending or receiving data. State signals $S_0, S_1,$ and $S_2,$ along with SYNC inform the peripheral circuitry of the state of the processor.

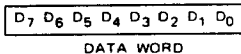
V_{CC} +5V \pm 5%

V_{DD} -9V \pm 5%

INSTRUCTION SET

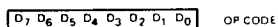
Data and Instruction Formats

Data in the 8008 is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

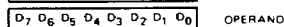
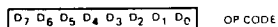


The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

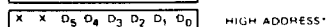
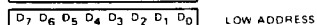
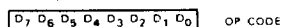
One Byte Instructions



Two Byte Instructions



Three Byte Instructions



TYPICAL INSTRUCTIONS

Register to register, memory reference, I/O arithmetic or logical, rotate or return instructions

Immediate mode instructions

JUMP or CALL instructions

*For the third byte of this instruction, D₆ and D₇ are "don't care" bits.

For the MCS-8™ a logic "1" is defined as a high level and a logic "0" is defined as a low level.

Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE			DESCRIPTION OF OPERATION
		D ₇ D ₆	D ₅ D ₄ D ₃	D ₂ D ₁ D ₀	
(1) MOV r ₁ , r ₂	(5)	1 1	D D D	S S S	Load index register r ₁ with the content of index register r ₂ .
(2) MOV r, M	(8)	1 1	D D D	1 1 1	Load index register r with the content of memory register M.
MOV M, r	(7)	1 1	1 1 1	S S S	Load memory register M with the content of index register r.
(3) MVI r	(8)	0 0	D D D	1 1 0	Load index register r with data B . . . B.
MVI M	(9)	0 0	1 1 1	1 1 0	Load memory register M with data B . . . B.
JNR r	(5)	0 0	D D D	0 0 0	Increment the content of index register r (r ≠ A).
DCR r	(5)	0 0	D D D	0 0 1	Decrement the content of index register r (r ≠ A).

Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

ADD r	(5)	1 0	0 0 0	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADD M	(8)	1 0	0 0 0	1 1 1	
ADI	(8)	0 0	0 0 0	1 0 0	
ADC r	(5)	1 0	0 0 1	S S S	Add the content of index register r, memory register M, or data B . . . B from the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ADC M	(8)	1 0	0 0 1	1 1 1	
ACI	(8)	0 0	0 0 1	1 0 0	
SUB r	(5)	1 0	0 1 0	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUB M	(8)	1 0	0 1 0	1 1 1	
SUI	(8)	0 0	0 1 0	1 0 0	
SBB r	(5)	1 0	0 1 1	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBB M	(8)	1 0	0 1 1	1 1 1	
SBI	(8)	0 0	0 1 1	1 0 0	

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE						DESCRIPTION OF OPERATION
		D ₇ D ₆	D ₅ D ₄ D ₃	D ₂ D ₁ D ₀				
ANA r	(5)	1 0	1 0 0	S S S				Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
ANAM	(8)	1 0	1 0 0	1 1 1				
ANI	(8)	0 0	1 0 0	1 0 0				
XRA r	(5)	1 0	1 0 1	S S S				Compute the EXCLUSIVE OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
XRAM	(8)	1 0	1 0 1	1 1 1				
XRI	(8)	0 0	1 0 1	1 0 0				
ORA r	(5)	1 0	1 1 0	S S S				Compute the INCLUSIVE OR of the content of index register r, memory register m, or data B . . . B with the accumulator.
ORAM	(8)	1 0	1 1 0	1 1 1				
ORI	(8)	0 0	1 1 0	1 0 0				
CMP r	(5)	1 0	1 1 1	S S S				Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CMPM	(8)	1 0	1 1 1	1 1 1				
CPI	(8)	0 0	1 1 1	1 0 0				
RLC	(5)	0 0	0 0 0	0 1 0				Rotate the content of the accumulator left.
RRC	(5)	0 0	0 0 1	0 1 0				Rotate the content of the accumulator right.
RAL	(5)	0 0	0 1 0	0 1 0				Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0	0 1 1	0 1 0				Rotate the content of the accumulator right through the carry.

Program Counter and Stack Control Instructions

(4) JMP	(11)	0 1 B ₂ B ₂ X X	X X X B ₂ B ₂ B ₂ B ₃ B ₃ B ₃	1 0 0 B ₂ B ₂ B ₂ B ₃ B ₃ B ₃				Unconditionally jump to memory address B ₃ . . . B ₃ B ₂ . . . B ₂ .
(5) JNC, JNZ, JP, JPO	(9 or 11)	0 1 B ₂ B ₂ X X	0 C ₄ C ₃ B ₂ B ₂ B ₂ B ₃ B ₃ B ₃	0 0 0 B ₂ B ₂ B ₂ B ₃ B ₃ B ₃				Jump to memory address B ₃ . . . B ₃ B ₂ . . . B ₂ if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
JC, JZ, JM, JPE	(9 or 11)	0 1 B ₂ B ₂ X X	1 C ₄ C ₃ B ₂ B ₂ B ₂ B ₃ B ₃ B ₃	0 0 0 B ₂ B ₂ B ₂ B ₃ B ₃ B ₃				Jump to memory address B ₃ . . . B ₃ B ₂ . . . B ₂ if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
CALL	(11)	0 1 B ₂ B ₂ X X	X X X B ₂ B ₂ B ₂ B ₃ B ₃ B ₃	1 1 0 B ₂ B ₂ B ₂ B ₃ B ₃ B ₃				Unconditionally call the subroutine at memory address B ₃ . . . B ₃ B ₂ . . . B ₂ . Save the current address (up one level in the stack).
CNC, CNZ, CP, CPO	(9 or 11)	0 1 B ₂ B ₂ X X	0 C ₄ C ₃ B ₂ B ₂ B ₂ B ₃ B ₃ B ₃	0 1 0 B ₂ B ₂ B ₂ B ₃ B ₃ B ₃				Call the subroutine at memory address B ₃ . . . B ₃ B ₂ . . . B ₂ if the condition flip-flop is false, and save the current address (up one level in the stack.) Otherwise, execute the next instruction in sequence.
CC, CZ, CM, CPE	(9 or 11)	0 1 B ₂ B ₂ X X	1 C ₄ C ₃ B ₂ B ₂ B ₂ B ₃ B ₃ B ₃	0 1 0 B ₂ B ₂ B ₂ B ₃ B ₃ B ₃				Call the subroutine at memory address B ₃ . . . B ₃ B ₂ . . . B ₂ if the condition flip-flop is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
RET	(5)	0 0	X X X	1 1 1				Unconditionally return (down one level in the stack).
RNC, RNZ, RP, RPO	(3 or 5)	0 0	0 C ₄ C ₃	0 1 1				Return (down one level in the stack) if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
RC, RZ, RM, RPE	(3 or 5)	0 0	1 C ₄ C ₃	0 1 1				Return (down one level in the stack) if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0	A A A	1 0 1				Call the subroutine at memory address AAA000 (up one level in the stack).

Input/Output Instructions

IN	(8)	0 1	0 0 M	M M 1				Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1	R R M	M M 1				Write the content of the accumulator into the selected output port (RRMMM, RR / 00).

Machine Instruction

HLT	(4)	0 0	0 0 0	0 0 X				Enter the STOPPED state and remain there until interrupted.
	(4)	1 1	1 1 1	1 1 1				

NOTES

- (1) SSS = Source Index Register } These registers, r_i, are designated A(accumulator-000),
DDD = Destination Index Register } B(001), C(010), D(011), E(100), H(101), L(110).
- (2) Memory registers are addressed by the contents of registers H & L.
- (3) Additional bytes of instruction are designated by BBBBBBBB.
- (4) X = "Don't Care".
- (5) Flag flip-flops are defined by C₄C₃ - carry (00=overflow or underflow), zero (01=result is zero), sign (10=MSB of result is "1"), parity (11=parity is even).

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	-55°C to +150°C
Input Voltages and Supply Voltage With Respect to V _{CC}	+0.5 to -20V
Power Dissipation	1.0 W @ 25°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{DD} = -9V ± 5% unless otherwise specified. Logic "1" is defined as the more positive level (V_{IH}, V_{OH}). "0" is defined as the more negative level (V_{IL}, V_{OL}).

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
I _{DD}	AVERAGE SUPPLY CURRENT- OUTPUTS LOADED*		30	60	mA	T _A = 25°C
I _{LI}	INPUT LEAKAGE CURRENT			10	μA	V _{IN} = 0V
V _{IL}	INPUT LOW VOLTAGE (INCLUDING CLOCKS)	V _{DD}		V _{CC} -4.2	V	
V _{IH}	INPUT HIGH VOLTAGE (INCLUDING CLOCKS)	V _{CC} -1.5		V _{CC} +0.3	V	
V _{OL}	OUTPUT LOW VOLTAGE			0.4	V	I _{OL} = 0.44mA C _L = 200 pF
V _{OH}	OUTPUT HIGH VOLTAGE	V _{CC} -1.5			V	I _{OH} = 0.2mA

*Measurements are made while the 8008 is executing a typical sequence of instructions. The test load is selected such that at V_{OL} = 0.4V, I_{OL} = 0.44 mA on each output.

A.C. CHARACTERISTICS

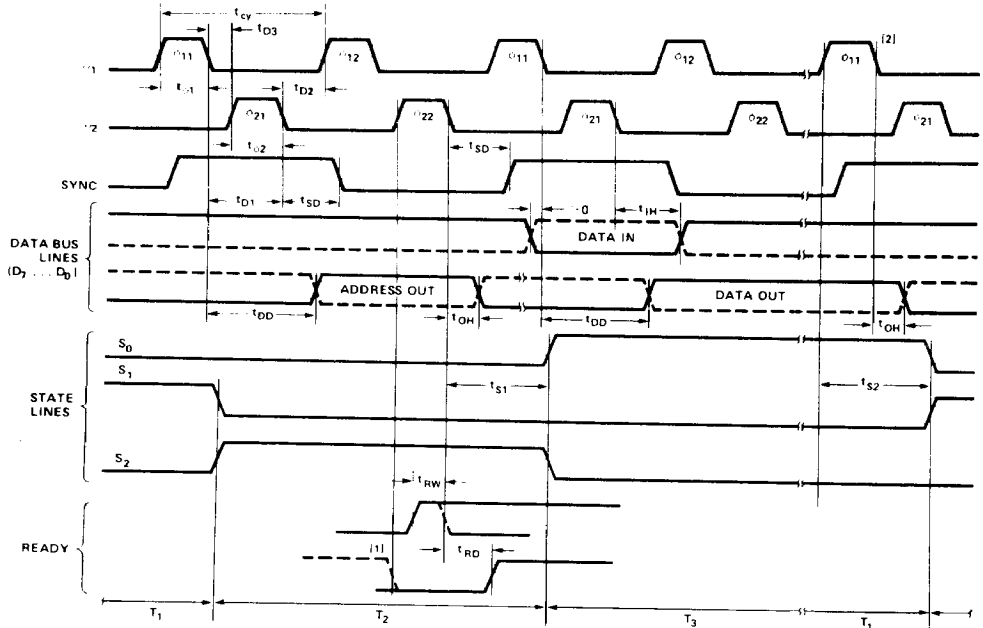
T_A = 0°C to 70°C; V_{CC} = +5V ± 5%, V_{DD} = -9V ± 5%. All measurements are referenced to 1.5V levels.

SYMBOL	PARAMETER	8008		8008-1		UNIT	TEST CONDITIONS
		LIMITS		LIMITS			
		MIN.	MAX.	MIN.	MAX.		
t _{CY}	CLOCK PERIOD	2	3	1.25	3	μs	t _R , t _F = 50ns
t _R , t _F	CLOCK RISE AND FALL TIMES		50		50	ns	
t _{φ1}	PULSE WIDTH OF φ ₁	.70		.35		μs	
t _{φ2}	PULSE WIDTH OF φ ₂	.55		.35		μs	
t _{D1}	CLOCK DELAY FROM FALLING EDGE OF φ ₁ TO FALLING EDGE OF φ ₂	.90	1.1		1.1	μs	
t _{D2}	CLOCK DELAY FROM φ ₂ TO φ ₁	.40		.35		μs	
t _{D3}	CLOCK DELAY FROM φ ₁ TO φ ₂	.20		.20		μs	
t _{DD}	DATA OUT DELAY		1.0		1.0	μs	C _L = 100pF
t _{OH}	HOLD TIME FOR DATA BUS OUT	.10		.10		μs	
t _{IH}	HOLD TIME FOR DATA IN	[1]		[1]		μs	
t _{SD}	SYNC OUT DELAY		.70		.70	μs	C _L = 100pF
t _{S1}	STATE OUT DELAY (ALL STATES EXCEPT T1 AND T11) [2]		1.1		1.1	μs	C _L = 100pF
t _{S2}	STATE OUT DELAY (STATES T1 AND T11)		1.0		1.0	μs	C _L = 100pF
t _{RW}	PULSE WIDTH OF READY DURING φ ₂₂ TO ENTER T3 STATE	.35		.35		μs	
t _{RD}	READY DELAY TO ENTER WAIT STATE	.20		.20		μs	

[1] t_{IH} MIN ≥ t_{SD}

[2] If the INTERRUPT is not used, all states have the same output delay, t_{S1}.

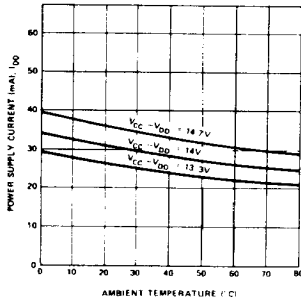
TIMING DIAGRAM



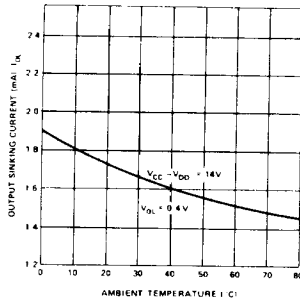
- Notes: 1. READY line must be at "0" prior to ϕ_{22} of T_2 to guarantee entry into the WAIT state.
 2. INTERRUPT line must not change levels within 200ns (max.) of falling edge of ϕ_1 .

TYPICAL D.C. CHARACTERISTICS

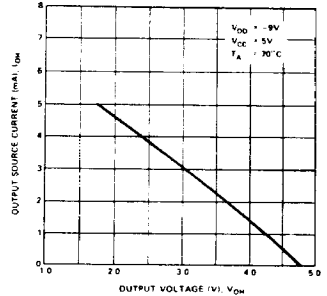
POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT SINKING CURRENT VS. TEMPERATURE

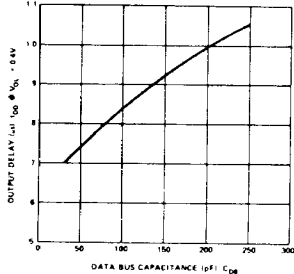


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



TYPICAL A.C. CHARACTERISTICS

DATA OUT DELAY VS. OUTPUT LOAD CAPACITANCE



CAPACITANCE $f = 1MHz$; $T_A = 25^\circ C$; Unmeasured Pins Grounded

SYMBOL	TEST	LIMIT (pF)	
		TYP.	MAX.
C_{IN}	INPUT CAPACITANCE	5	10
C_{DB}	DATA BUS I/O CAPACITANCE	5	10
C_{OUT}	OUTPUT CAPACITANCE	5	10